Progress Towards
Next Generation MRF Timing System

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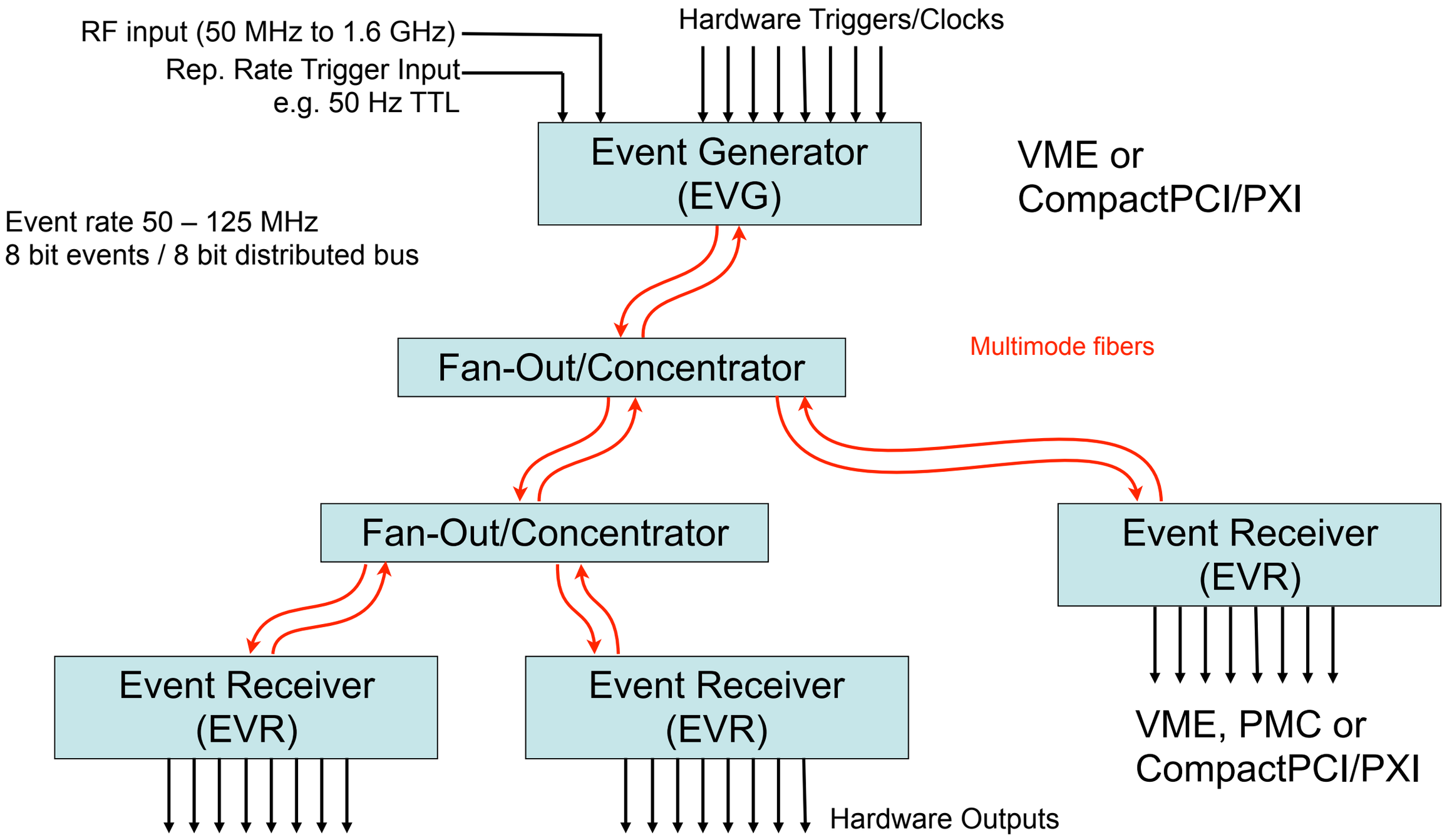
Current Event System Topology



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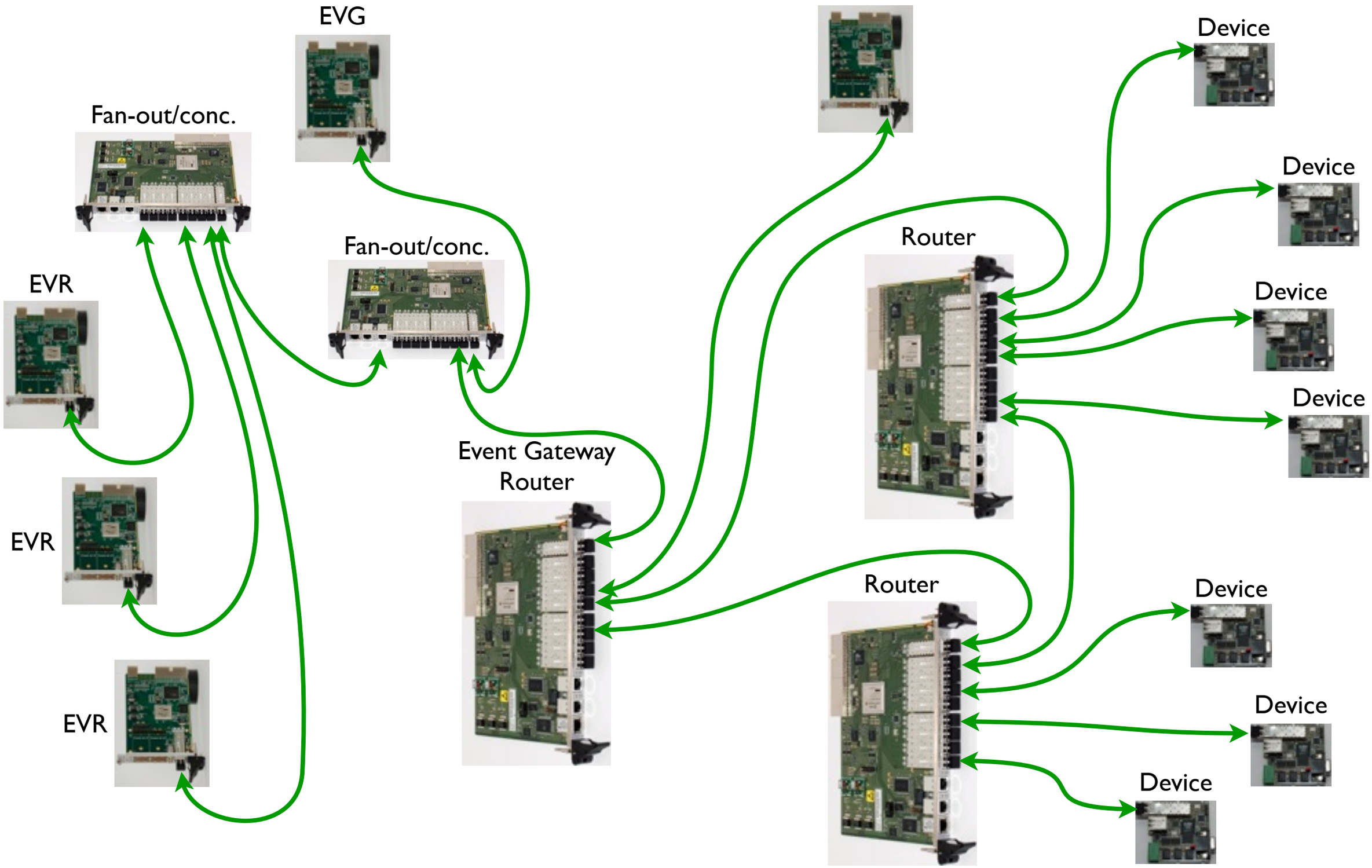
Timing/Data Network Topology (hybrid)
Presented in 2009 (no interest, not implemented)



Motivation for Change

- 142,8 MHz Event clock rate requirement (SwissFEL)
- 230 series VME EVG/EVR are based on “old” technology
- “no space left on device” (applies to VME-EVR, PMC-EVR)
- VME still going strong, requirement for update

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Higher Event Clock Rate

- One could think: “not a big deal”, FPGAs go well beyond 10 Gbit/s
- In reality “show stopper”, we need to be phase locked

- Current HW
  - limited by Fan-Out CDR bit rate of 2.7 Gbit/s (event clock 135 MHz), no alternatives available
  - Fan-Outs without CDR are not usable, multiple E/O, O/E conversions cause distortions and corrupt the event stream
  - Current VME hardware based on Virtex II Pro, max. rate 2.5 Gbit/s (event clock 125 MHz)
- The Clock and Data Recovery Circuit (CDR) does reconstruct the signal on the bit level with deterministic timing

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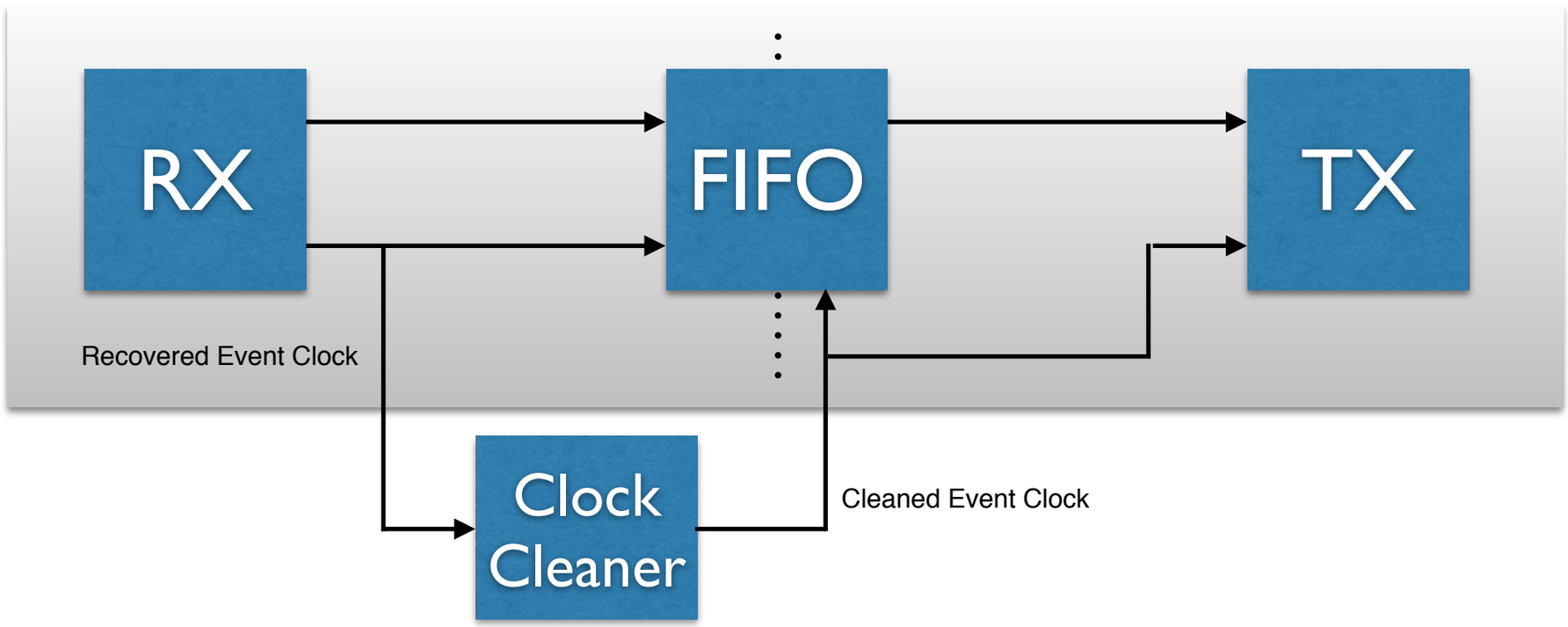
Solution

- We go deeper in signal recovery
- Event stream is decoded at every level in timing network and event clock is regenerated and cleaned
- The whole stream is regenerated
- Issue: how to maintain deterministic timing
  - Delay measurement



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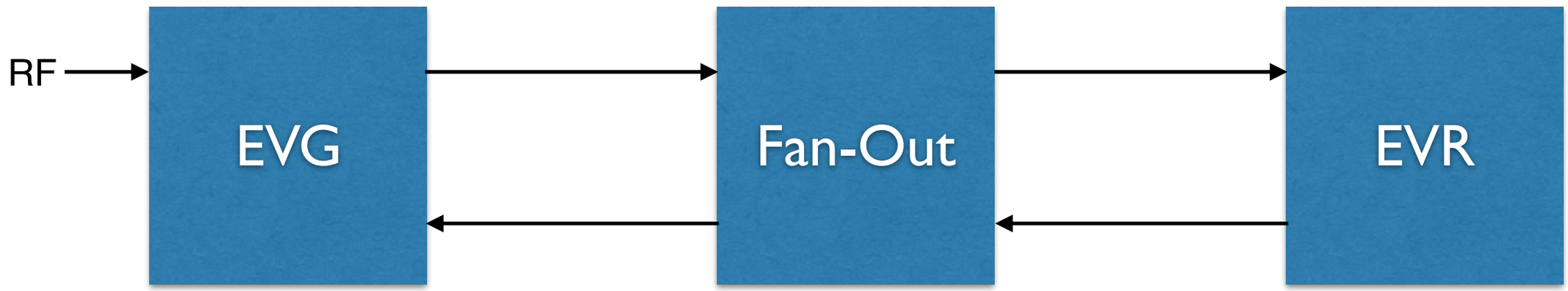
Delay Compensation



- EVG sends out delay “beacon” event regularly
- Beacon is received and sent back to EVG by Fan-Out
- EVG measures time delay between transmitted and received beacon event
- EVG embeds time delay result in transmitted event stream
- Fan-Out extracts incoming time delay value from incoming event stream
- Fan-Out monitors its internal delay + next fibre loop’s delay and adds this value to the received time delay value. The total delay is embedded in the stream and sent forward
- EVR buffers the received event stream and adjusts the buffer (FIFO) delay so that the buffer delay + received time delay value matches a programmed target delay
- Process is continuous

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Major Changes

- Support for higher event clock rate SwissFEL requirement 142,8 MHz
- Delay drift compensation
  - –requires changes to current protocol
  - –incompatibility with existing HW and/or firmware
  - –possible to produce gateway to hook up existing EVRs
- Supported platforms:
  - –VME (new designs for EVG, Fan-Out, EVR)
  - –PXIe (existing PXIe-EVR-300 HW with new FW)
  - –mTCA.4 (prototype in development, new FW)

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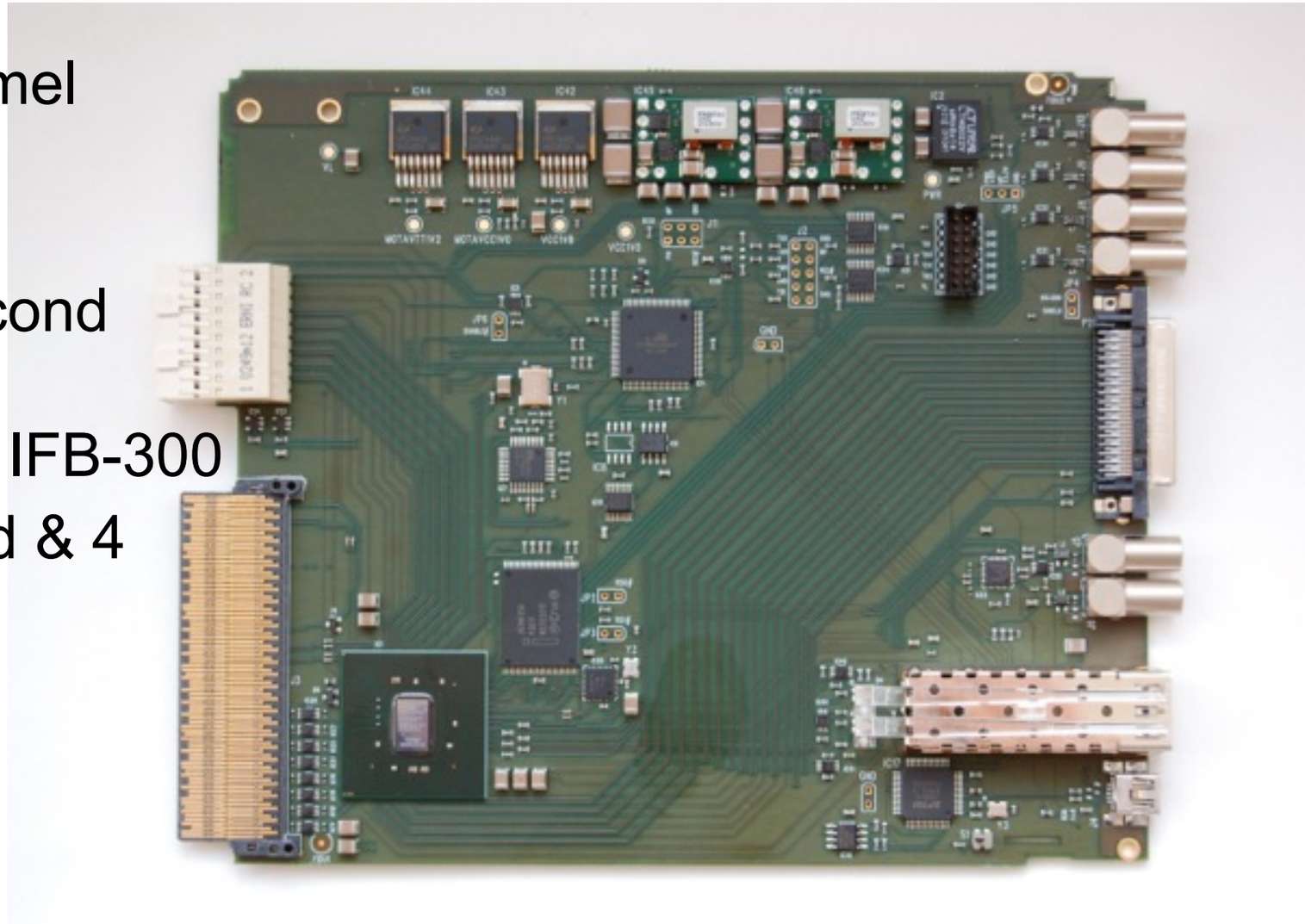
mTCA.4 EVR/EVG Prototype

- Xilinx Kintex-7 FPGA
- DESY based MMC using Atmel microcontroller
- 4 TTL Outputs
- 2 TTL Inputs (1 for EVG, second LEMO for RF input)
- microSCSI for Interface Box IFB-300
- mTCA.4 backplane 8 bussed & 4 PTP lines
- Support for rear I/O



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Hardware Considerations

- Current thoughts:
  - Make EVG/Fan-Out based on same hardware
  - reduce one fan-out level (EVG would have 8 TX ports)
  - option of providing RF reference to fan-outs to minimise jitter in timing network
- Initially EVG/Fan-Out form factor VME
  - does not rule out other form factors, however, so far other form factors have not been considered

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Further Improvements for Next Generation

- Current issues:
  - Unplugging the fibre does currently cause a burst of spurious events
    - adding a small buffer (and some delay) will allow the detection of a link break down before events are decoded
  - Current VME-EVR-230RF requires “tuning” to match the operating conditions
    - delay compensation will remove this requirement

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Hardware Requests / Interests?

- New VME form factor
  - drop ethernet interface
  - firmware upgrades through VME bus