Components for Integrating Device Controllers for Fast Orbit Feedback

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Topics

- PMC-SFP Module for Diamond Fast Orbit Feedback
- Future plans upgrading PMC-SFP module
- Backward Channel for Timing System
- Running EPICS/RTEMS on modified VME-EVR

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PMC-SFP for Diamond Fast Orbit Feedback

- Xilinx Virtex II Pro FPGA XC2VP30-6 FPGA
- 64 Mbytes (32M x 16 bit) SDRAM
- Four SFP (Small Form factor Pluggable) transceivers
- Fractional clock synthesizer
- PLX PCI9030 32-bit PCI I/O Accelerator
- XCF16P Platform Flash for configuration

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Diamond Firmware for PMC-SFP

- PMC-SFP mounted on MVME5500 SBCs is reponsible for receiving data from the BPMs and passing the data further to the FB processor
- No feedback processing (matrix multiplication, filtering) in FPGA firmware
- Diamond is currently using following FPGA (XC2VP30) resources:
  - 22% Slices
  - 20% of internal BRAM
  - Four RocketIOs
  - No PPC, No multipliers
- FPGA firmware developed at Diamond – Diamond open to share code with other institutes when a ”Memorandum of Understanding” exists

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PMC-SFP PCI Data Transfer

- Diamond requirement: 2 kbytes in 50 us
- PLX PCI9030 32-bit PCI I/O Accelerator
  - 32-bit, 33 MHz PCI
  - Target only: no mastering DMA capability
- Work-around: DMA controller on MVME5500 can do burst reads and achieve read data transfer rate of 40 us for 2 kbytes approx. 50 Mbyte/s

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Initial plans for upgraded PMC-SFP

- Xilinx Virtex II Pro FPGA XC2VP30-6 FPGA
- 64 Mbytes (32 x 16 bit) SDRAM
- Four SFP transceivers
- Fractional clock synthesizer
- Replace PLX PCI9030 32-bit PCI I/O Accelerator with PLX 9656
  - 64-bit, 66 MHz PCI
  - Local bus remains 60 MHz, 32-bit
  - Master/DMA capability
  - Allows for higher data transfer bandwidth e.g. on x86 based HW

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Alternate plans for upgraded PMC-SFP

- More changes?
- Virtex 5 LXT instead of Virtex II Pro?
  - Latest technology
  - PCI Express endpoint in fabric (e.g. MicroTCA)
  - PowerPC (Virtex 5 FXT) not available yet
- Real requirements:
  - FPGA resources
  - Feedback algorithm in FPGA firmware?
  - Do we need SDRAM/DDR?
  - Do we need a CPU?
  - I/O or other peripherals
  - Form factor: PMC?

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Timing System Backward Transmission Channel

- Traditionally events, distributed bus signals and data transfered only from EVG to EVR
- Converting the fan-out modules into fan-out – concentrators events etc. can be sent from EVRs towards the EVG
- Backward events:
  - EVR hardware trigger input
  - EVR software event
  - Concentrators forward events (FIFO)
- Backward distributed bus data (8 bits wide):
  - Source: EVR hardware input
  - DBUS data OR'ed together by concentrators
- Data transfer:
  - Limited size software data buffer from EVRs towards EVG

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Fan-out Concentrator Hardware

- 6U CompactPCI form factor
- Xilinx XC5VLX50T FPGA
- Nine SFP transceivers:
  - 1 to 8 fan-out, 8 to 1 concentrator
  - Cross-point switches to allow for
    - Fan-out operation: direct path from RX to TXn
    - GTP connection: each transciver is connected to FPGA
- PCI interface
- Microcontroller/10baseT interface for standalone operation
- Prototype hardware will be available by the end of 2007

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EPICS/RTEMS on VME Event Receiver

- Hardware VME-EVR-230 with following additions:
  - 128 Mbytes (32M x 32 bit) of SDRAM
  - Micrel KSZ8841 10/100 MAC/PHY
  - XC2VP20 instead of XC2VP7
- RTEMS-4.7.99.2
- Modified virtex BSP
  - Existing driver for opb_uartlite, opb_interrupt
- Network driver for Micrel KSZ8841 10/100 MAC/PHY

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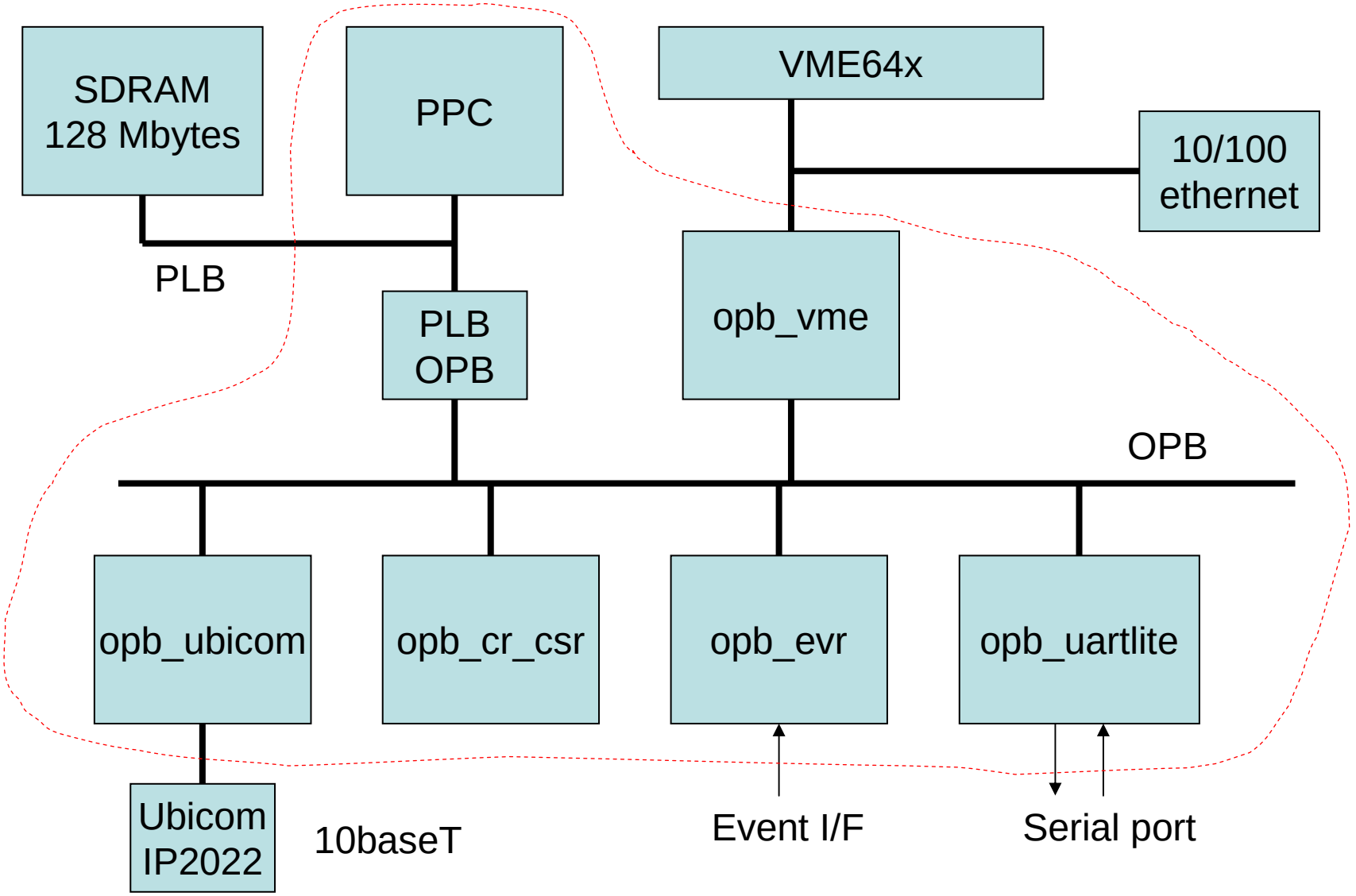
FPGA Firmware Structure



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Experience during porting

- Prebuilt tools for RTEMS easy to set up
- Issues with Xilinx debugging tools
  - Reliability problems with powerpc-eabi-gdb
  - Difficult to debug:
    - PowerPC stops responding after accessing an invalid address
- Linker script problem with virtex BSP
- **environ was allocated but not assigned

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EPICS/RTEMS on VME Event Receiver TODO

- Boot code to load application into SDRAM
  - Bootloader in ISOCM
- VME driver (VME is already available on OPB)
- Improve performance (enable caching)

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