Timing System with Two-Way Signalling

cRIO-EVR

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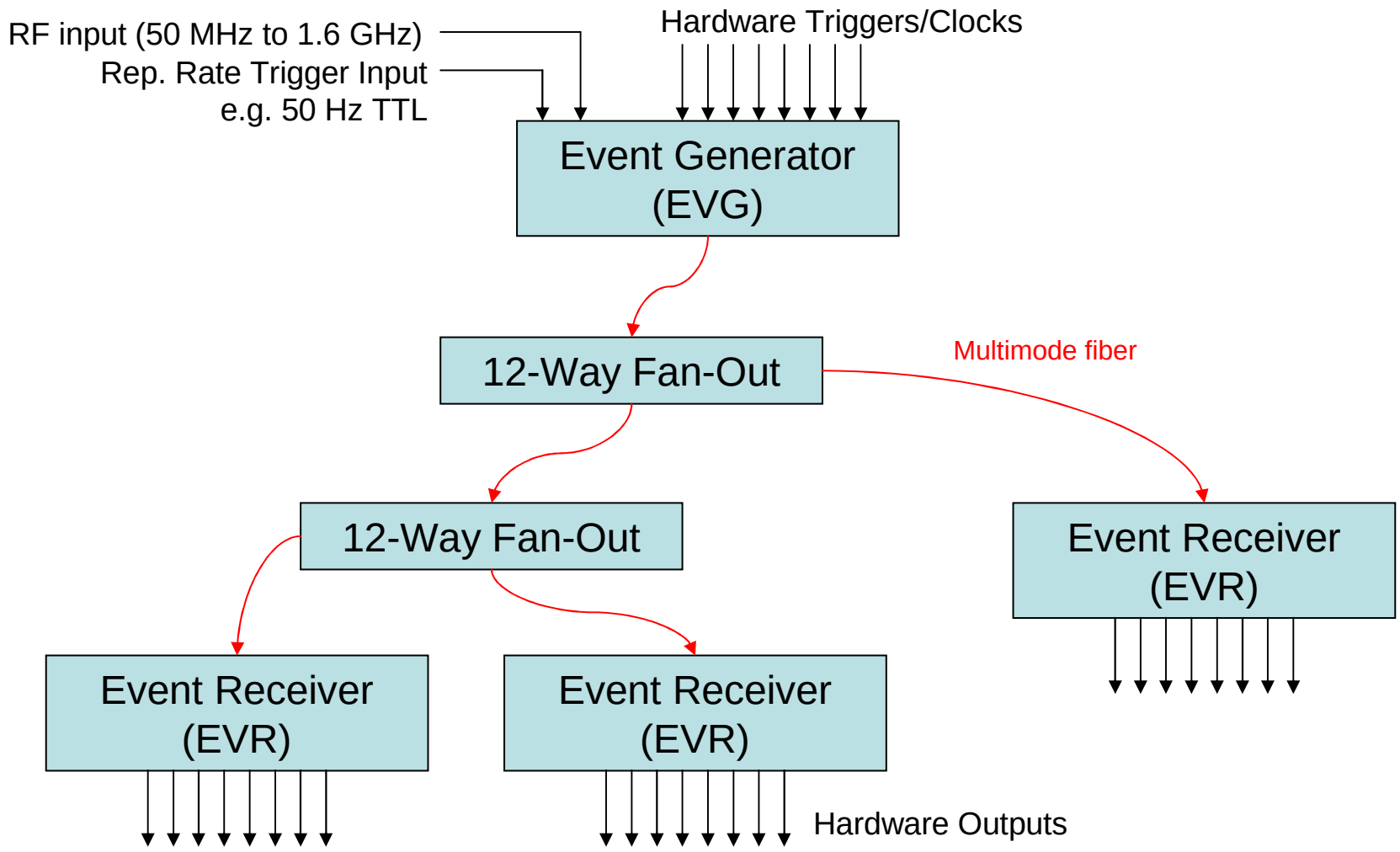
Timing System Topology



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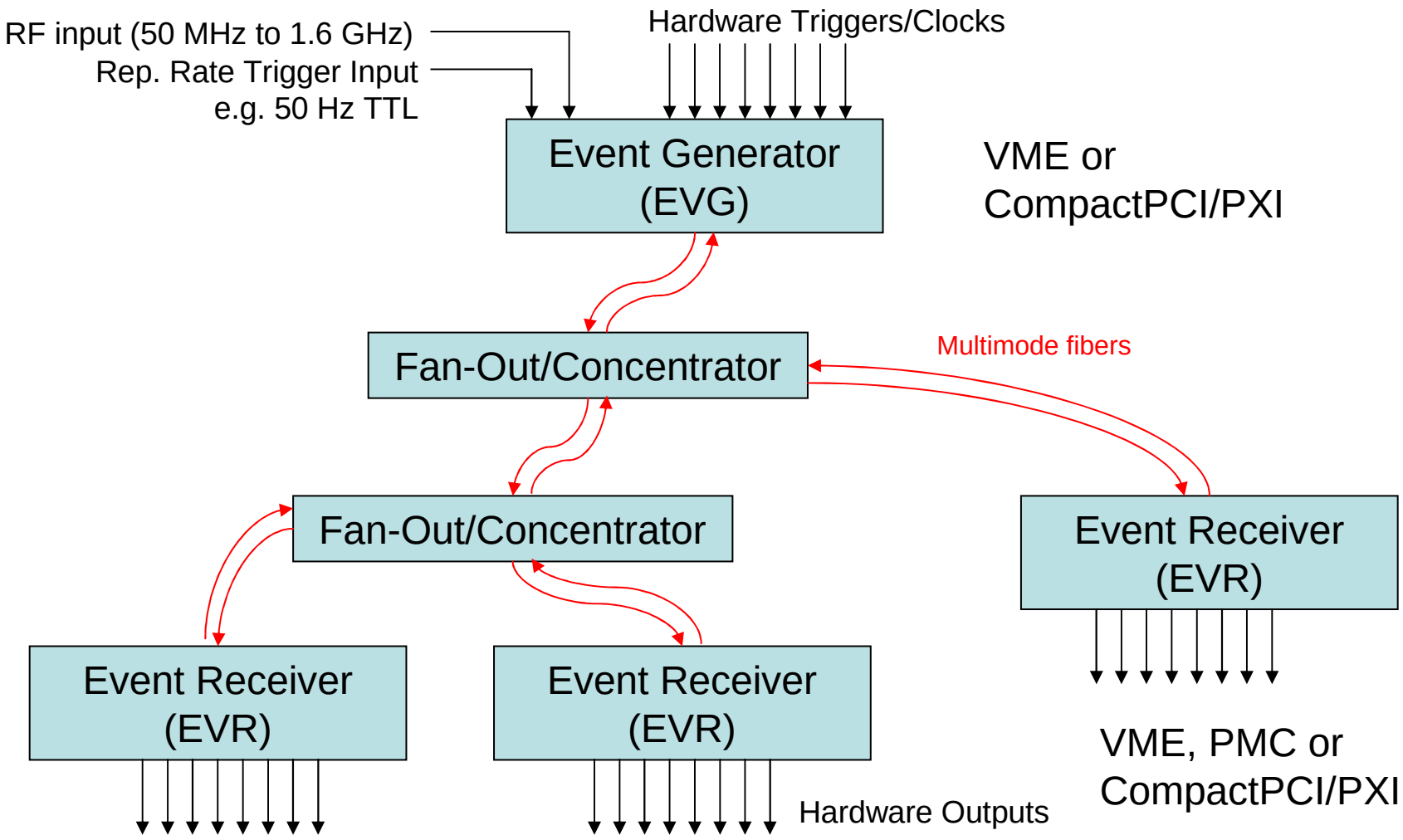
Two-Way Signalling



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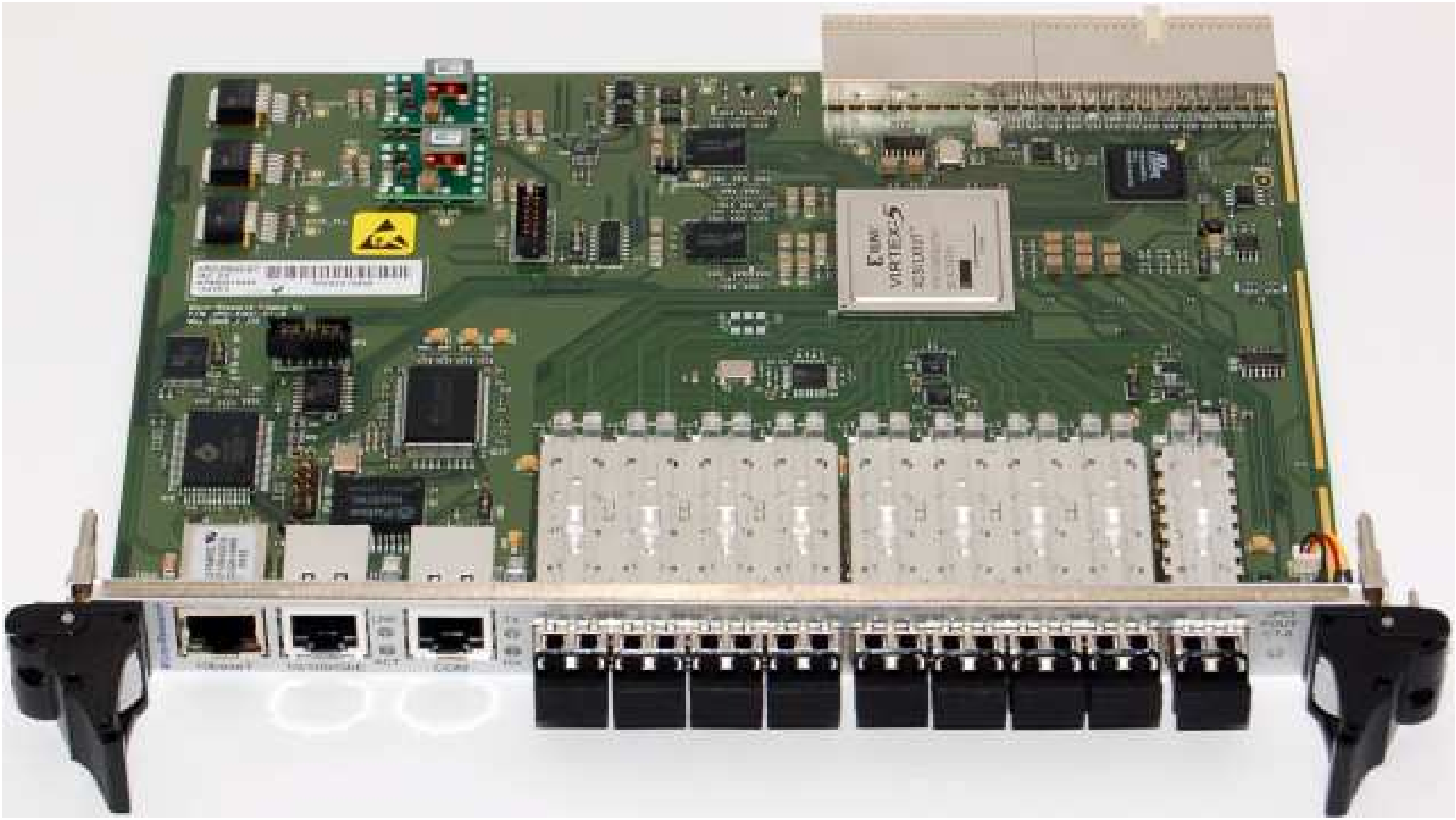
cPCI-FCT-8



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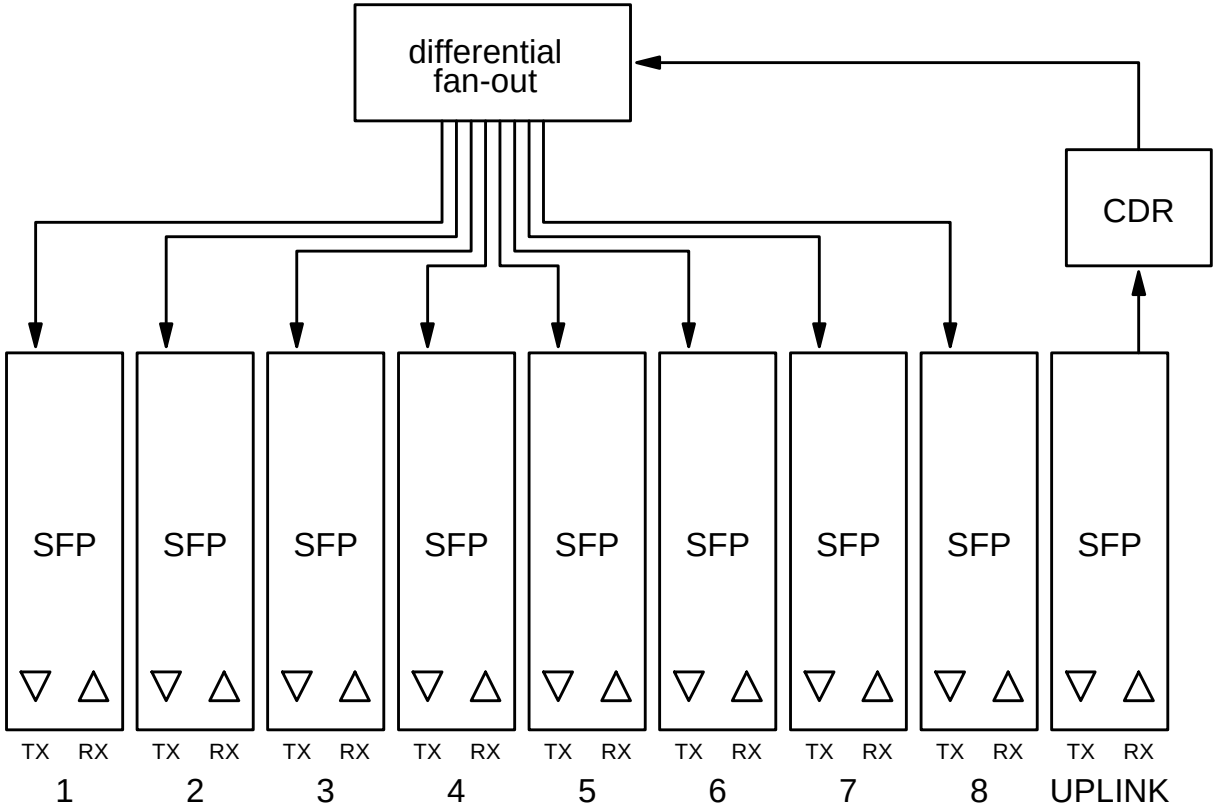
Fan-Out

- one in – eight out fan-out
- up to 2.5 Gbps SFPs with multimode transceivers (single mode for extended reach)
- CDR to regenerate gigabit rate signal



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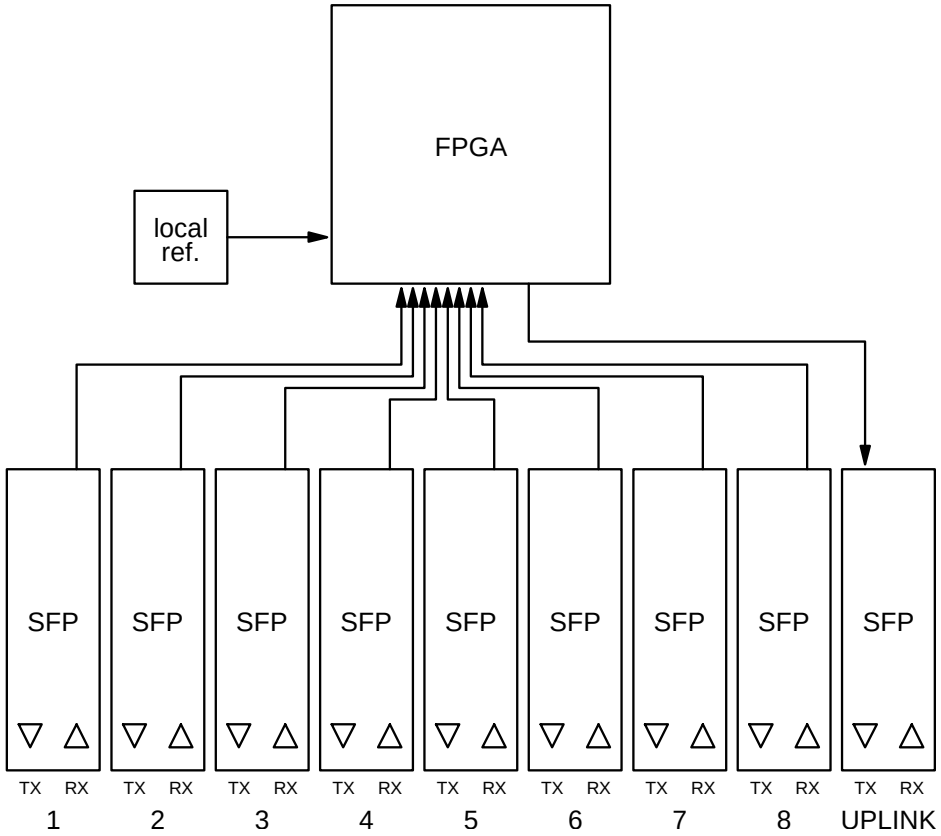
Concentrator

- Eight in – one out
- Uplink TX port is using local reference



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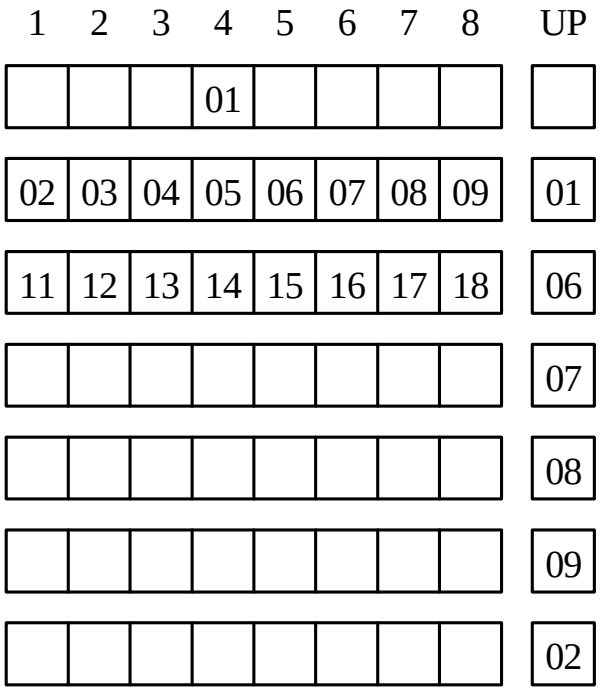
Concentrator – Event Forwarding

- Each RX channel has 2k event FIFO
  - Hold events in case of simutananeous events from several ports
- Priority encoding
  - First come – first served
  - Round-robin
    - One event from one port

    → next port



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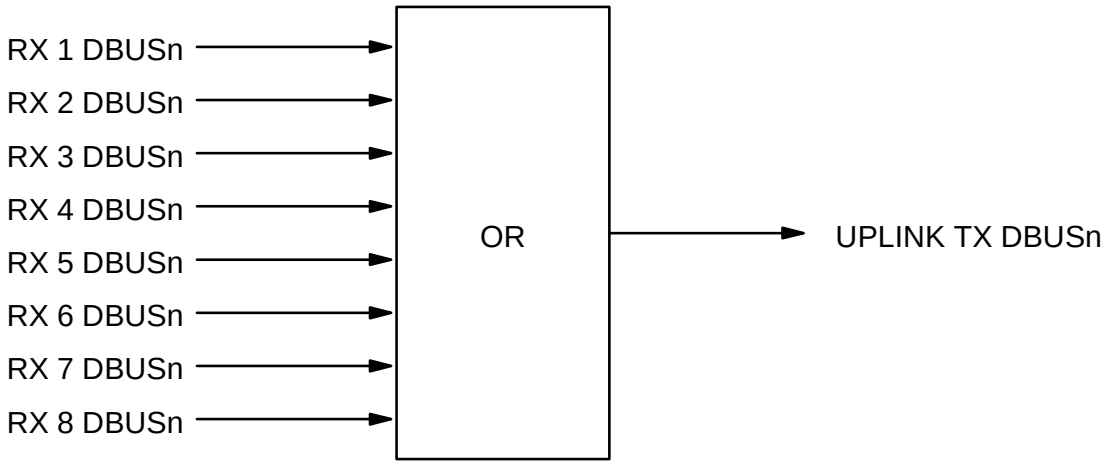
Concentrator – Distributed bus bits

- Eight bit wide distributed bus
- Each distributed bus bits from all ports is logically OR'ed together



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Concentrator – Data Buffer Forwarding

- Each RX channel has 2 kbyte data FIFO
- Forwarding starts immediately after start of reception
  - Latency is minimized
- Priority: Round-Robin

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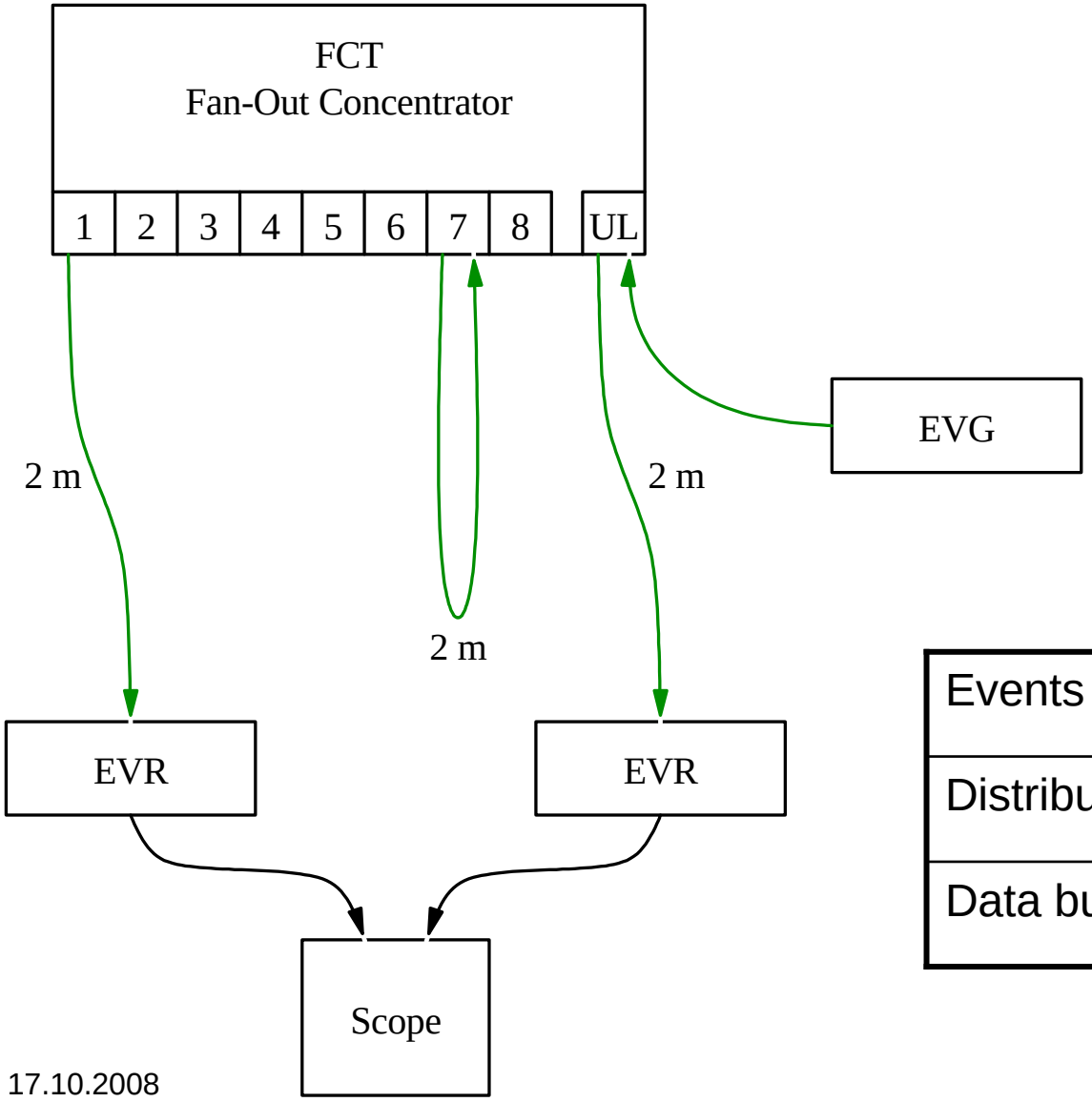
Concentrator – Latency Performance



- 499.654/4 MHz Event Clock
- Latency of Concentrator only (without fibre delays)

Events	162 ± 4 ns
Distributed bus bits	107 ± 4 ns
Data buffers	181 ± 8 ns

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CompactRIO Event Receiver

- Timing receiver form factors:
  - VME64x 6U
  - PMC (PCI mezzanine)
  - CompactPCI/PXI 3U
- Need for timing for embedded systems
- MRF is working together with LANL and NI to design an Event Receiver for cRIO

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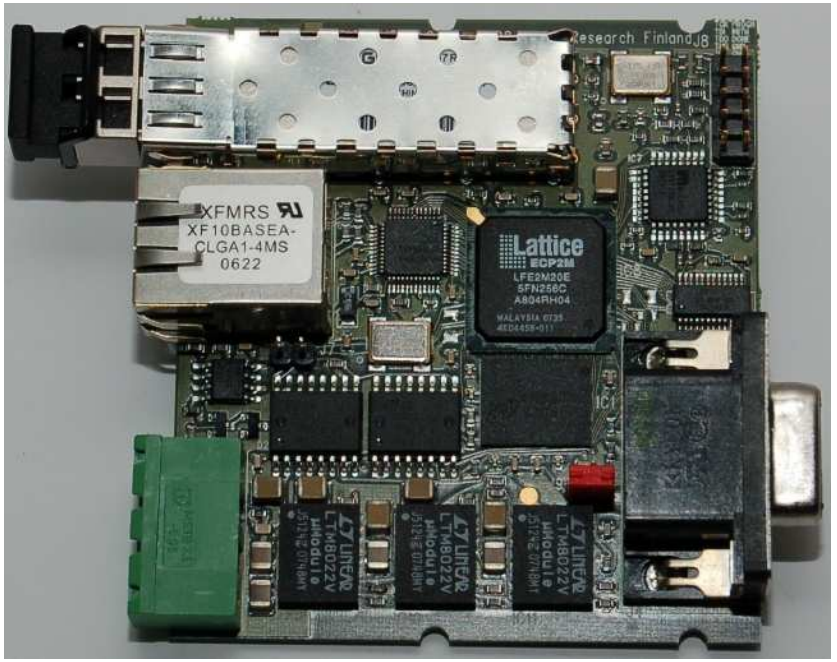
CompactRIO EVR prototype

- SFP transceiver for event link
- FPGA with high speed serial link
- 10/100 ethernet for control and configuration
- 64 Mbytes DDR2 memory
- 2 × 16 Mbits serial flash
- EEPROM
- 9 to 35 VDC power supply input



Challenges (when used with NI HW/LabView)

- Power dissipation
- Achieve required timing resolution
- Achieve required data transfer capability
- Control and configuration methods
  - cRIO
  - ethernet

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cRIO-EVR Stand-alone

- Lattice Mico32 (lm32) system
  - 32-bit soft-core CPU
  - 10/100 ethernet MAC
  - DDR2 memory controller
- 9 to 35 VDC power supply input
- DSUB15 with max. 11 I/O pins
- Work going on to port RTEMS to lm32 target

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