Latest Timing System Developments

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Register Map Changes (new register mapping)

- CompactPCI boards implement new register mapping
  - Direct addressing of registers, sequencer memories, etc.
  - Register space has grown to 64 kbytes
  - One type of EVR pulse generator:
    - Registers for delay, width, prescaler with SW probable width
    - No more different types of outputs: PDP, OTP, TEV, LVL
  - 128 bit wide mapping RAM:
    - 32 bits reserved for internal functions, heartbeat, fifo event, etc.
    - 32 bits for triggering pulses
    - 32 bits to set pulse output
    - 32 bits to reset pulse output
    - No overlapping mapping bits
  - Mapping registers for HW inputs and outputs
  - EVG interrupt support
  - EVR Upstream signaling
- Available for PMC-EVR
- Will be available for VME versions later

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Event Mapping RAM

Event code	Internal func.	Pulse trigger	Pulse set	Pulse clear
1				
2				
…				
255				

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Register Map Changes

- VHDL package defines EVR construction
  - Number of front panel I/O
  - Number of Universal I/O modules
  - Backplane I/O
  - Number of pulse generators (max. 32)
  - Pulse delay and width extents
- Same VHDL sources for all form factors

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VHDL package for cPCI-EVR

```
-- Event Receiver configuration parameters
 -- C_EVR_PULSE_GENS sets the number of internal pulse generators
 constant C_EVR_PULSE_GENS    : integer := 10;
 constant C_EVR_TTL_INPUTS    : integer := 2;
 -- C_EVR_TTL_OUTPUTS defines the number of front panel TTL outputs
 constant C_EVR_TTL_OUTPUTS   : integer := 0;
 -- C_EVR_CML_OUTPUTS defines the number of front panel CML outputs
 -- note: the CML output mapping registers are appended after the
 -- TTL output mapping registers
 constant C_EVR_CML_OUTPUTS   : integer := 0;
 -- C_EVR_UNIV_OUTPUTS defines the number of Universal outputs
 -- = twice the number of Universal I/O slots
 constant C_EVR_UNIV_OUTPUTS  : integer := 10;
 constant C_EVR_UNIV_INPUTS   : integer := 10;
 -- C_EVR_GPIOS defines the number of GP I/Os in Universal I/O slots
 constant C_EVR_GPIOS         : integer := 8;
 -- C_EVR_TB_OUTPUTS defines the number of Transition Board/Rear I/O/
 -- PXI star trigger/trigger bus outputs
 constant C_EVR_TB_OUTPUTS    : integer := 0;
```


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VHDL package for cPCI-EVR (cont.)

```
-- C_EVR_PRESCALERS defines the number of prescalers
constant C_EVR_PRESCALERS    : integer := 3;
constant C_EVR_PULSE_PRESC_RANGE : integer_array(0 to C_EVR_PULSE_GENS-1)
:= (16, 16, 16, 16,  0,  0,  0,  0,  0,  0);
constant C_EVR_PULSE_DELAY_RANGE : integer_array(0 to C_EVR_PULSE_GENS-1)
:= (32, 32, 32, 32, 32, 32, 32, 32, 32, 32);
constant C_EVR_PULSE_WIDTH_RANGE : integer_array(0 to C_EVR_PULSE_GENS-1)
:= (32, 32, 32, 32, 16, 16, 16, 16, 16, 16);
constant C_EVR_PRESC_RANGE : integer_array(0 to C_EVR_PRESCALERS-1)
:= (16, 16, 16);
constant C_EVR_MICREL_WORD   : std_logic_vector := X"0C928166";
constant C_EVR_USEC_DIVIDER  : std_logic_vector := X"007D";
constant C_EVR_USE_TRANSMITTER : boolean := TRUE;
-- C_EVR_ENABLE_BACKWARD_CHANNEL enables EVR event transmission and
-- disables loopback of received event stream
constant C_EVR_ENABLE_BACKWARD_CHANNEL : boolean := TRUE;
```


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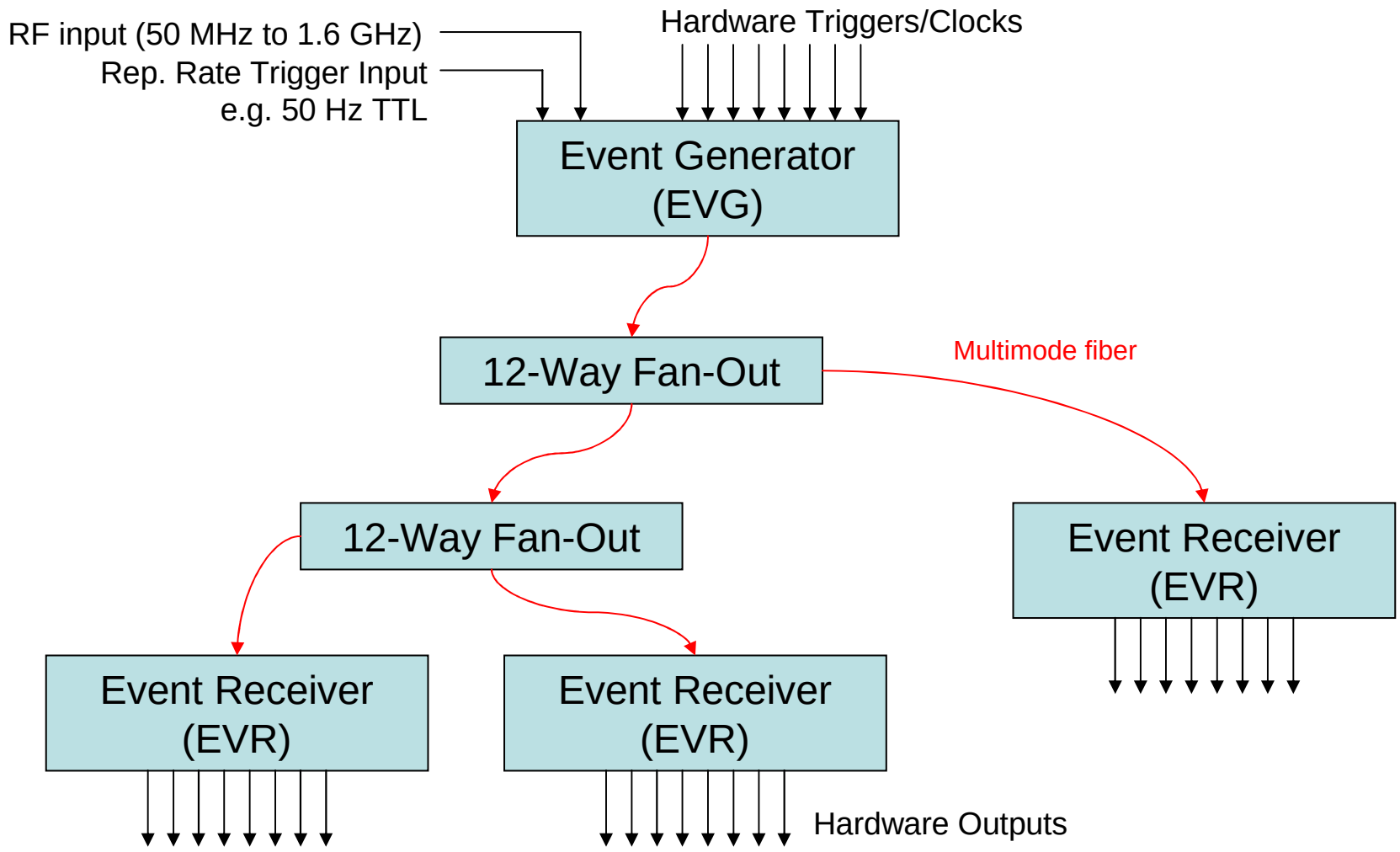
Downstream Timing



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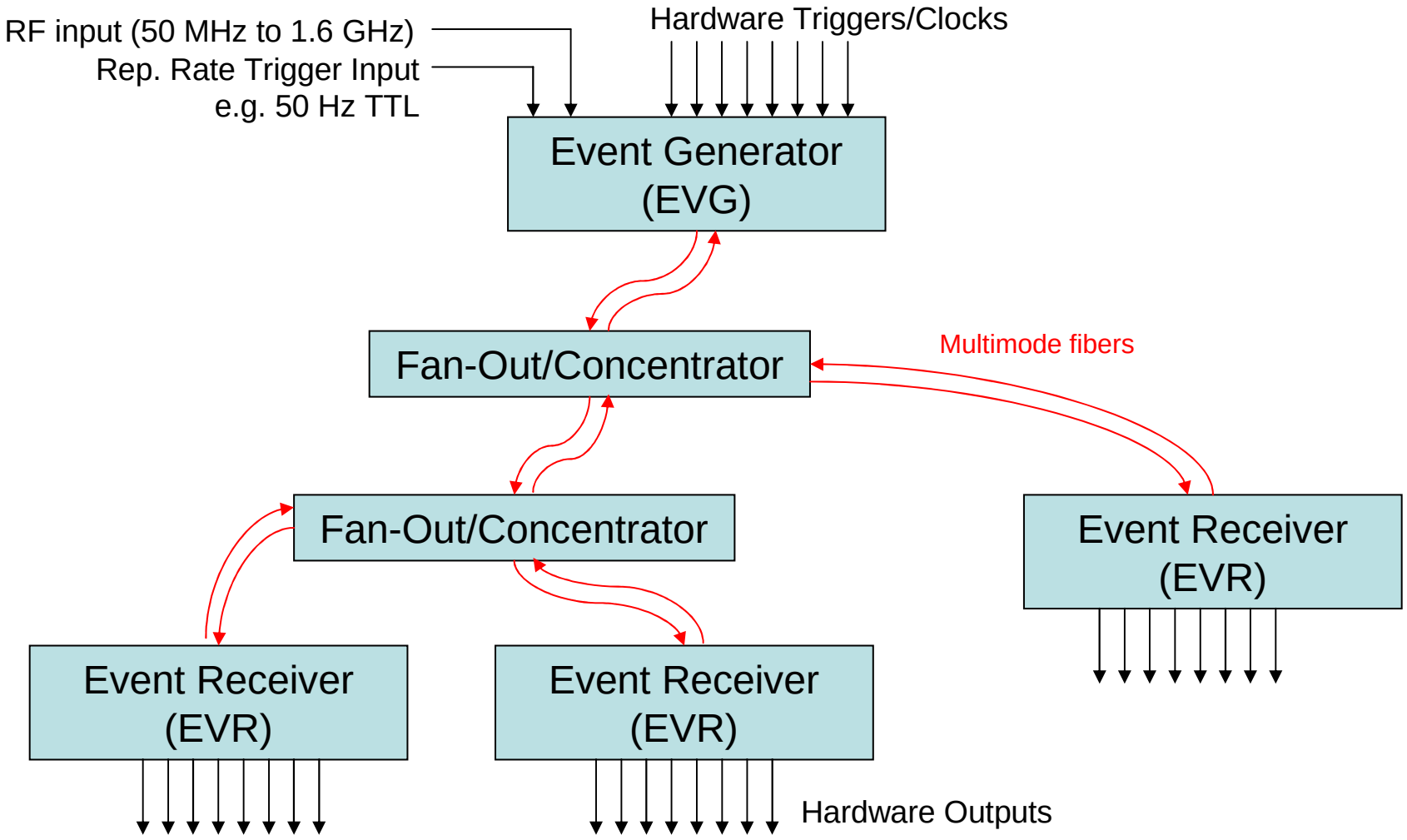
Timing System with Upstream



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Advantages of an upstream timing channel

- Event driven system, 255 event codes
- Events are sent out with the event clock rate which is derived from an external RF reference
- Event clock rate 50 to 125 MHz
- Events generated
  - From external HW inputs
  - Two sequencers (up to 2048 events/sequencer)
  - Multiplexed counters
  - Software
- Eight distributed bus signals, updated simultaneously at the event clock rate, no interference with events
- Event Generators may be cascaded
  - EVGs synchronized to different clocks

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Timing System Features (cont.)

- Event Receivers lock to the EVG event clock and generate
  - pulse outputs with programmable delay and width
  - level outputs
  - Software interrupts
  - Synchronous clocks
  - RF recovery (VME-EVR-230RF only)
- Support for Timestamping/distribution of time
- Timestamping of external events
- Data transfer support with predictable timing
  - Up to 2 kbyte buffer
  - Max. 62.5 Mbytes/s
- SFP transceivers, multi-mode fiber

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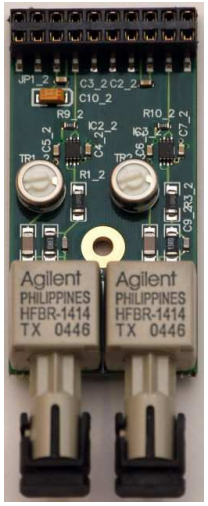
Universal I/O Modules

- 25.4 mm x 52 plug-in units
- two outputs or inputs each
- can be fitted on VME-EVG-230 and VME-EVR-230(RF), VME-UNIV-TB, CompactPCI EVG/EVR, CompactPCI side-by-side module
- Module specification available on-line for custom module development

Optical HFBR-1414	Optical HFBR-1528	NIM Output	TTL Output	TTL Input	LVPECL Output	LVPECL Output
						
820 nm	650 nm 1 mm POF					10 ps step Delay tuning

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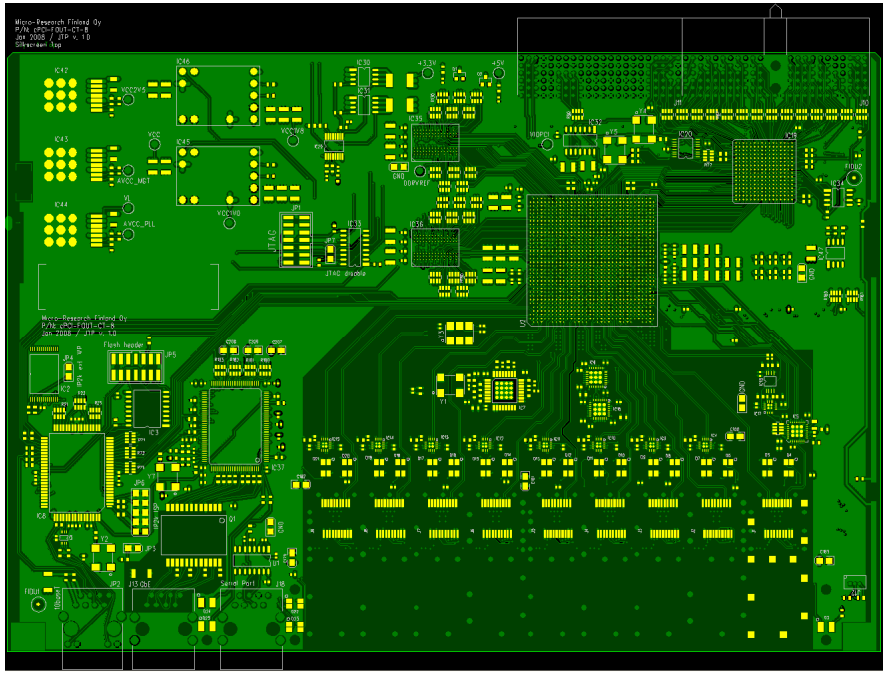
Fan-Out Concentrator Module (cPCI-FOUT-CT-8)



- Upstream events
- Upstream distributed bus
- Upstream data transfer
- Fiber length measurement

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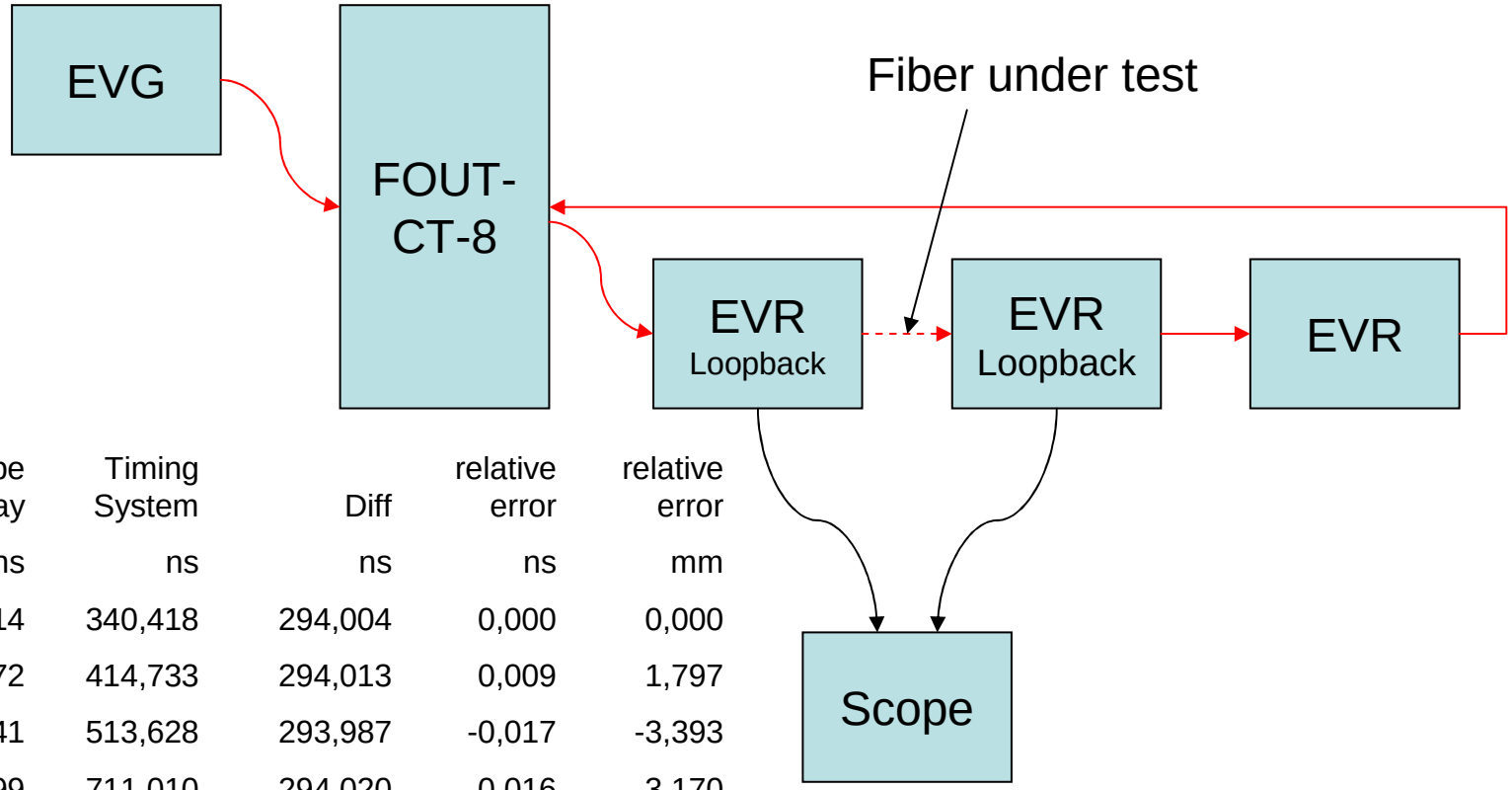
Fiber Delay Measurement Setup



Fiber length	Scope Delay	Timing System	Diff	relative error	relative error
m	ns	ns	ns	ns	mm
9	46,414	340,418	294,004	0,000	0,000
24	120,72	414,733	294,013	0,009	1,797
44	219,641	513,628	293,987	-0,017	-3,393
84	416,99	711,010	294,020	0,016	3,170
164	812,625	1106,629	294,004	-0,001	-0,105
294	1455,446	1749,457	294,011	0,007	1,340
554	2741,692	3035,692	294,000	-0,005	-0,930

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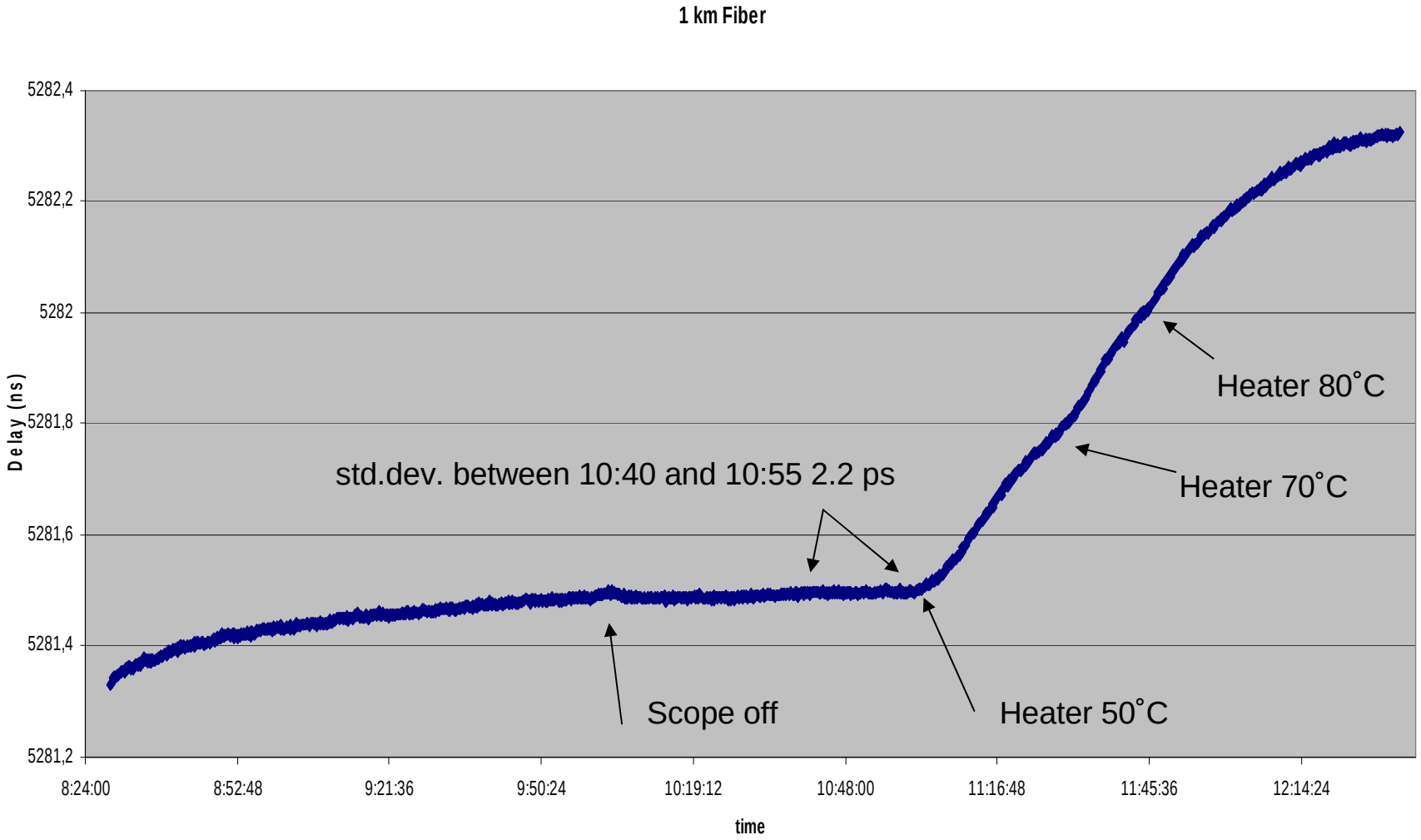
Fiber Delay Measurement



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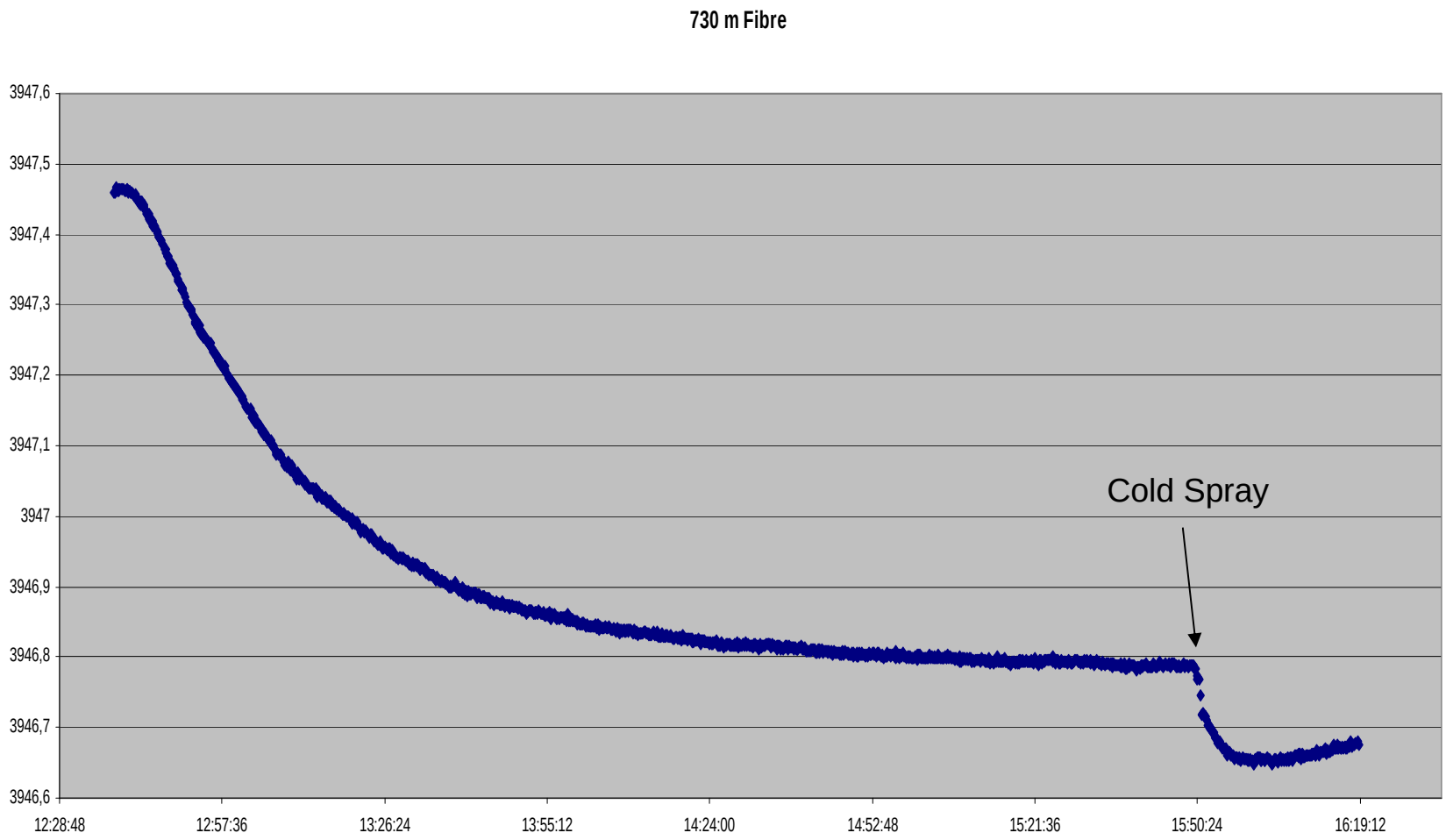
Fiber Delay Measurement



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Form Factors

- Event Generator
  - VME64x
  - PXI/CompactPCI
- Event Receiver
  - VME64x
  - PMC
  - PXI/CompactPCI
  - Future form factors:
    - CompactRIO (National Instruments)?
    - EPIC form factor? (see http://www.pc104.org)
      - Integrated CPU (either soft-CPU inside FPGA or Freescale Coldfire)
      - Integrated EVR
      - PC104 bus / PCI bus
    - uTCA?

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Future Interests

- EPIC form factor EVR prototype (see http://www.pc104.org)
  - Integrated CPU (either soft-CPU inside FPGA or Freescale Coldfire)
  - Integrated EVR
  - PC104 bus / PCI bus
- Event Receiver for CompactRIO (National Instruments)
  - Feasibility? cRIO interface not very suitable for timing receiver

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