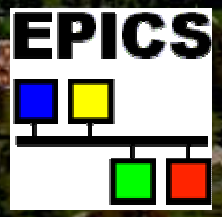
An Accelerator Timing Receiver for CompactRIO

Jukka Pietarinen

NI Week 2008 – Big Physics Symposium
August 2008

Introduction

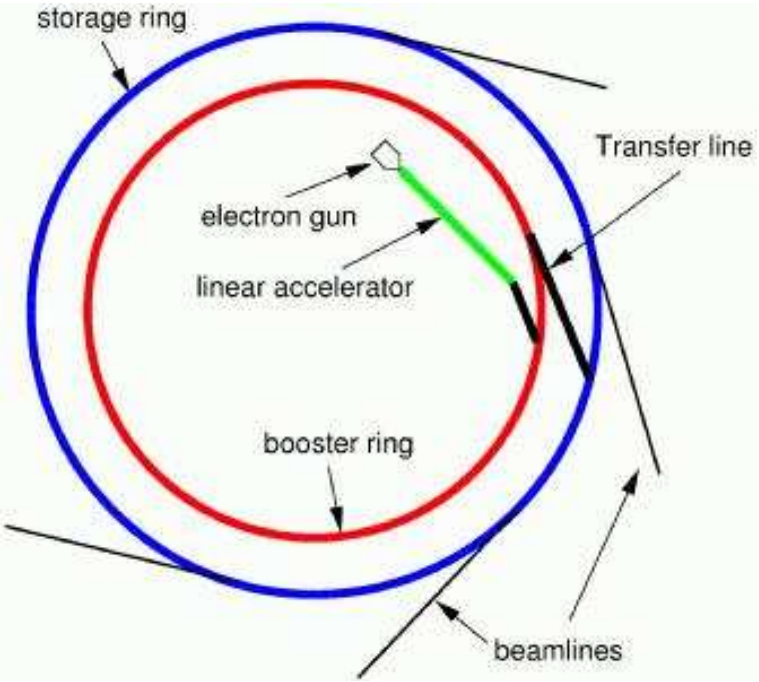


- Timing System originally developed for synchrotrons
- First user Swiss Light Source, Paul-Scherrer Institut
- Users include:
  - Diamond Light Source Ltd., U.K.
  - SSRF, Shanghai, China
  - ASP, Australia
  - ALBA, Spain (Tango)
  - Elettra, Trieste, Italy (Tango)
  - BEPCII, Insitute for High Energy Physics, Beijing, China
  - LCLS, Stanford Linear Accelerator Center, USA
  - SNS, Oak Ridge National Laboratory, USA
  - And others...
- Most sites run EPICS (Experimental Physics and Industrial Control System) see http://www.aps.anl.gov/epics/

Photo provided by Diamond Light Source Ltd

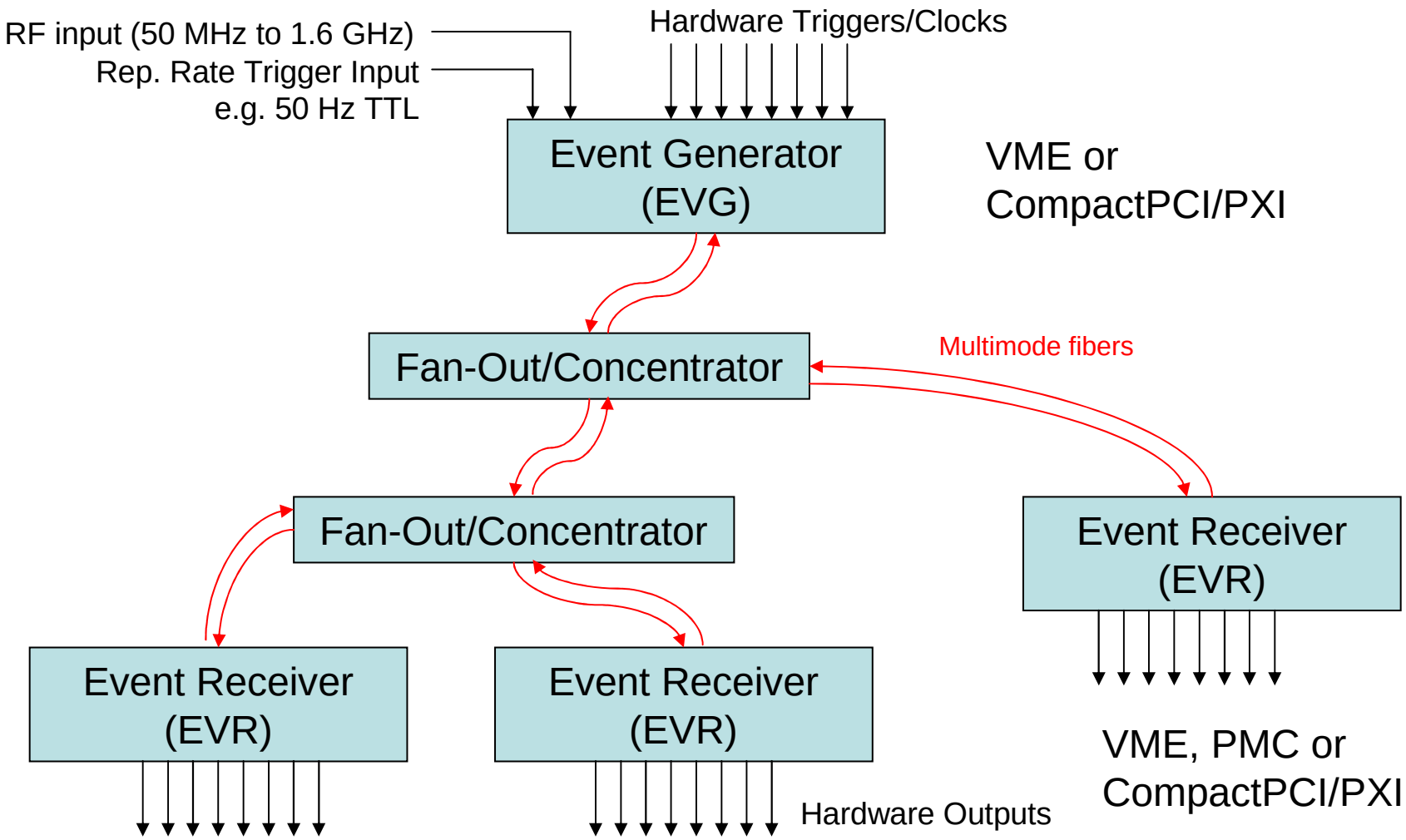
Complete Timing System

- Injection timing
  - Electron Gun triggering
  - Kicker Magnet control
  - Target individual RF buckets
- Clock distribution e.g.
  - Storage Ring revolution clock
  - Booster revolution clock
- Accelerator Time delivery
  - Timestamping of events
- Beamline timing
  - Provide beam timing for experiments
- Deterministic Data Transmission
  - E.g. Beam flavor



jukka.pietarinen@mrf.fi

Timing System Topology



jukka.pietarinen@mrf.fi

CompactRIO Event Receiver

- Timing receiver form factors:
  - VME64x 6U
  - PMC (PCI mezzanine)
  - CompactPCI/PXI 3U
- Need for timing for embedded systems
- MRF is working together with LANL and NI to design an Event Receiver for cRIO

jukka.pietarinen@mrf.fi

Event Receiver Performance

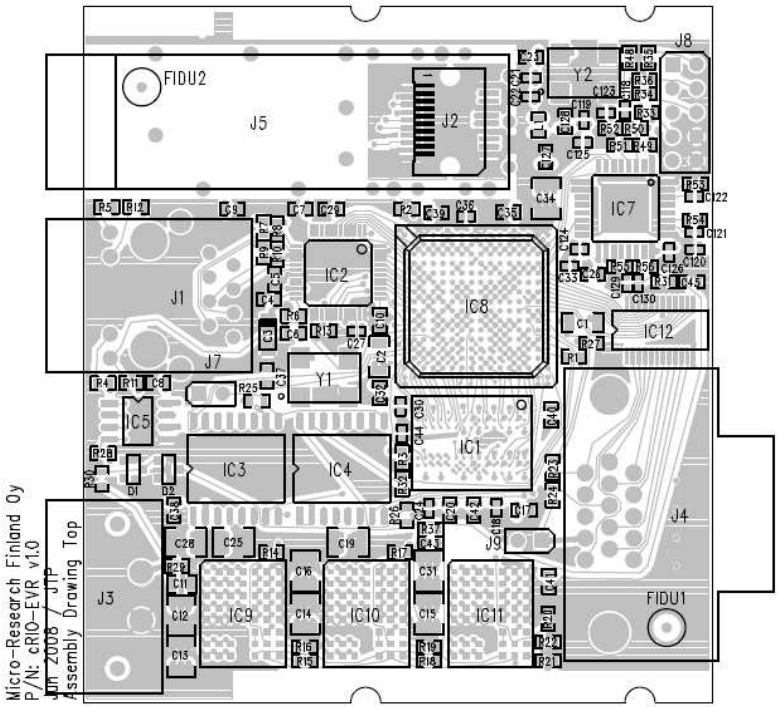
Module	Resolution	Jitter typ.
VME-EVR-230	8 ns min. *)	< 25 ps RMS
VME-EVR-230RF (standard outputs)	8 ns min. *)	< 15 ps RMS
VME-EVR-230RF (CML outputs)	400 ps (8 ns / 20)	< 5 ps RMS
cPCI-EVR-220	10 ns min.	< 25 ps RMS
cPCI-EVR-230 PMC-EVR-230	8 ns min. *)	< 25 ps RMS
cRIO-EVR	TBD Target < 1 μs	TBD Target < 10 ns RMS

*) 10 ps with UNIV-LVPECL-DLY module

jukka.pietarinen@mrf.fi

CompactRIO EVR prototype

- SFP transceiver for event link
- FPGA with high speed serial link
- 10/100 ethernet for control and configuration
- 64 Mbytes DDR2 memory
- 2 × 16 Mbits serial flash
- EEPROM
- 9 to 35 VDC power supply input



Challenges

- Power dissipation
- Achieve required timing resolution
- Achieve required data transfer capability
- Control and configuration methods
  - cRIO
  - ethernet

jukka.pietarinen@mrf.fi

Further Information

Internet: http://www.mrf.fi
Email: jukka.pietarinen@mrf.fi

EPICS: http://www.aps.anl.gov/epics/