ICALEPCS San Francisco 2013 Timing Workshop

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Topics

- Form factors
- Firmware changes
- Event / Link rate
- Other requests

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Form Factors

	EVG	EVR	Fan-Out
VME	x	x	x
PMC		x	
CompactPCI 3U	x	x	
CompactPCI 6U	x	x	x
PCI Express		x	
PXI Express 3U	x	x	
microTCA.4			

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PXIe-EVG-300 Design - Features

- Basically same functionality as earlier CompactPCI modules have
- New event clock sources:
  - 10 MHz PXI clock multiplied by 10
  - 100 MHz PXIe clock
- In addition to
  - Front panel RF input with divider
  - Fractional synthesizer

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Future Form Factors?

- microTCA.4 (SLAC, ESS among others)
  – in development, prototype by end of 2013

- LANSCE has selected to use VPX as platform
  – any other users for VPX?

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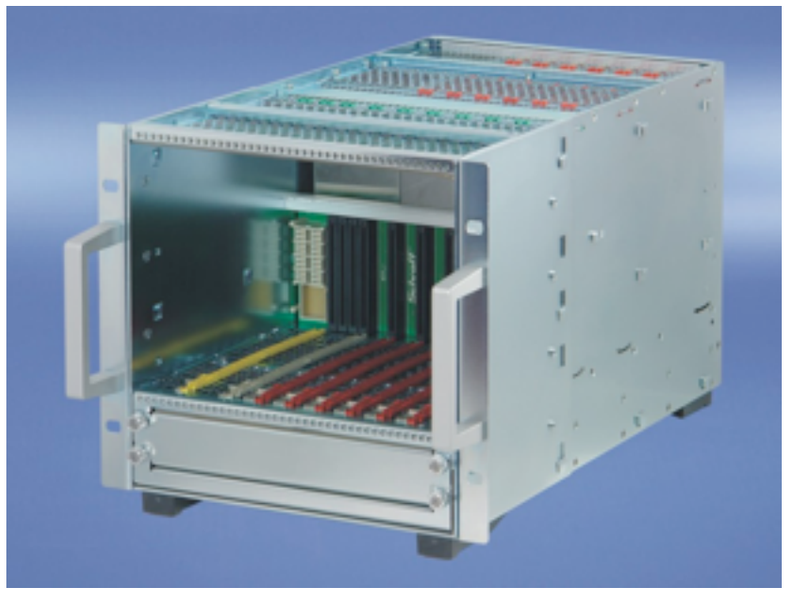
MTCA.4



Schroff MicroTCA.4 cube

- 180.6 mm x 148.5 mm PCB size
- High speed point-to-point links for e.g. PCI Express on backplane
- radial clocks TCLKA, TCLKB, TCLKC, TCLKD point to point connection through MCH
- eight M-LVDS bus lines e.g. for triggers, gates or slow clocks
- Rear transition module with direct connection to front board

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MTCA.4 Event Receiver (in development)

- radial clocks TCLKA, TCLKB, TCLKC, TCLKD point to point connection through MCH + redundant MCH
- eight M-LVDS bus lines
- LVDS signals to uRTM
- six front panel LEMOs (two input, four output)
- front panel micro-SCSI connector for I/O interface board with eight Universal I/O slots
- Option for routing signals through the back using an uRTM with micro-SCSI connector
- Based on Xilinx Kintex FPGA

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What is VPX (VITA 46)?

- VITA standard
- 3U / 6U form factor
- new connector for switched fabrics (PCI Express etc.)
- rugged - designed with (moving) defense applications in mind
- Supports PMC and XMC
- Standard allows for lots of different (incompatible) configurations
- Rear I/O
- No timing on backplane

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Future Form Factors?

- Form factors needing upgrade
  - VME
  - PMC -> XMC
  - VPX form factor could be implemented with upgraded PMC/XMC EVR and transition module designed for VPX

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EVR Firmware changes available currently only for cPCI-EVR(TG)-300

- Motivation: ELI requirement to distribute clocks
  - 0.5 Hz, 1 Hz, 10 Hz, 100 Hz, 1 kHz, 2 kHz, 100 kHz, 200 kHz
- Number of EVR prescalers 3 -> 8
- Prescalers are synchronized by “reset prescaler” event sent from EVG sequencer every 2 s
- EVR Pulse generators can be triggered from
  - Distributed bus signals
  - EVR Prescalers

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Event Link rate

- Current limit 2.5 Gbps / 125 MHz
  - Virtex II Pro (VME, PMC, cPCI 3U)
  - Fan-Out limit 2.7 Gbps

- Need for new Fan-Out
  - Requests: (remote) diagnostics, optical powers etc.
  - Form factor? VME / cPCI / uTCA.4?

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Other Requests?

- Single Linux kernel driver to cover all event hardware
  - has to cover different PCI / PCI Express chip sets
  - major differences in
    - interrupt handling
    - firmware upgrades

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