MRF Timing System with Active Delay Compensation

Motivation for Active Delay Compensation

- Requirement for higher event rate
  - SwissFEL event clock rate is 142.9 MHz, 7 ns event clock cycle
- Current fan-out CDR technology limits event clock rate to 135 MHz
- No commercial CDR solution available
- Need to make fan-outs active

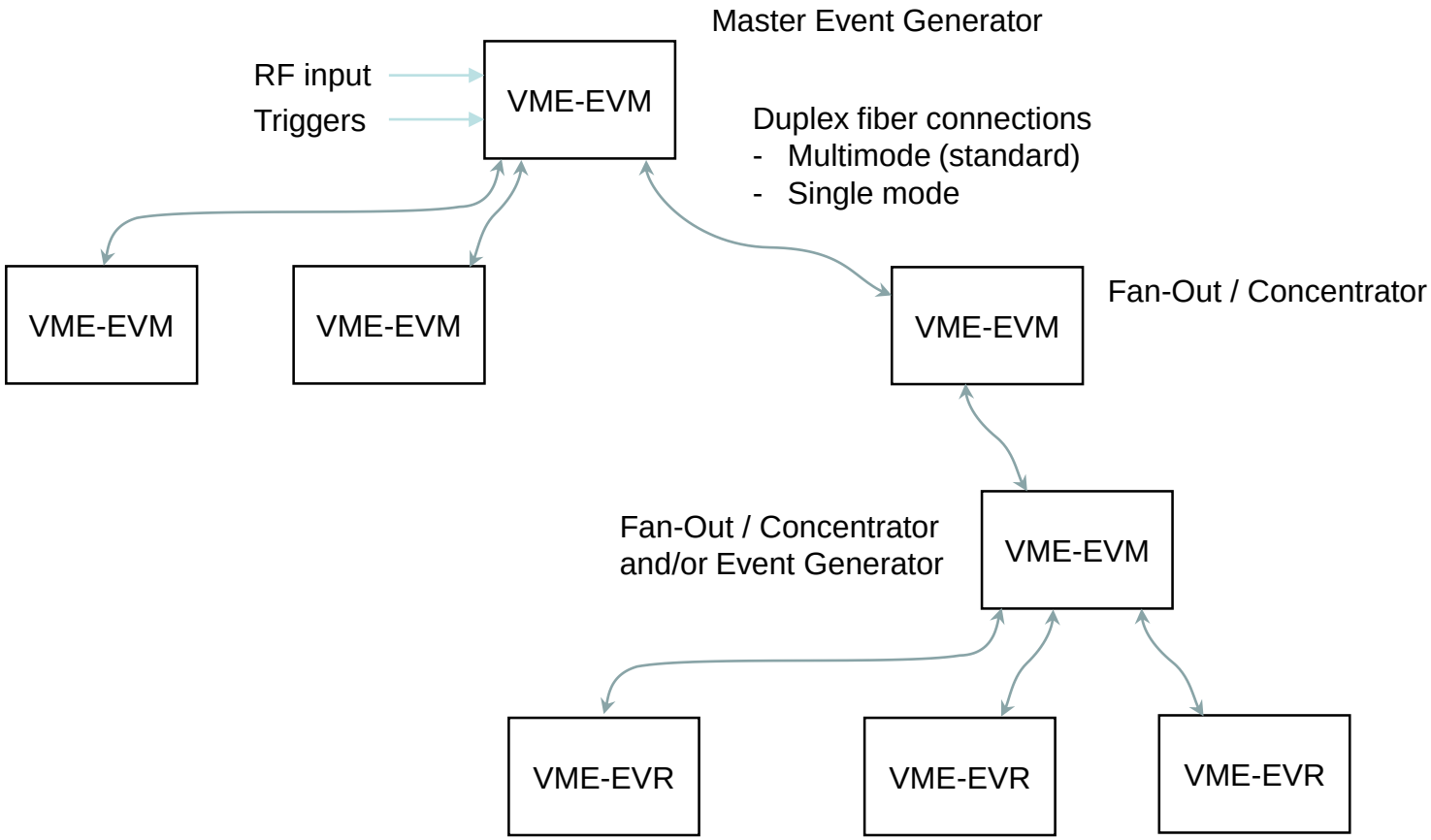
- Adds fan-out complexity and cost
- Incompatibility with existing HW/FW (work-around using compensation up to last stage fan-out and new FW)

+ Compensation for delay drift
+ Adds possibility to fine tune all triggers of a single receiver
+ Precise synchronization of downstream EVGs

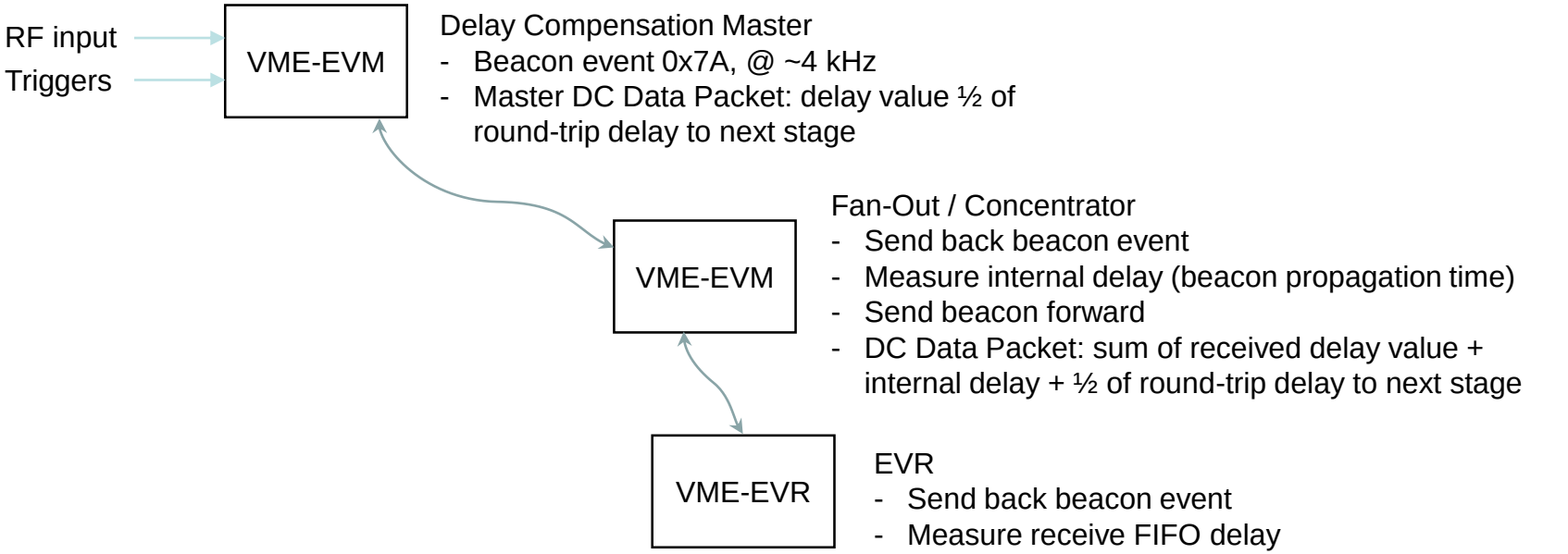
Hardware Compatibility with Delay Compensation

- VME-EVM-300 (new product combines EVG and Fan-Out/Concentrator)
- VME-EVR-300 (new product)
- PCIe-EVR-300 (limited support, low delay compensation accuracy, suited mainly as software interface or pulses not requiring sub-ns accuracy)
- mTCA-EVR-300 (in development, estimated availability early 2016)

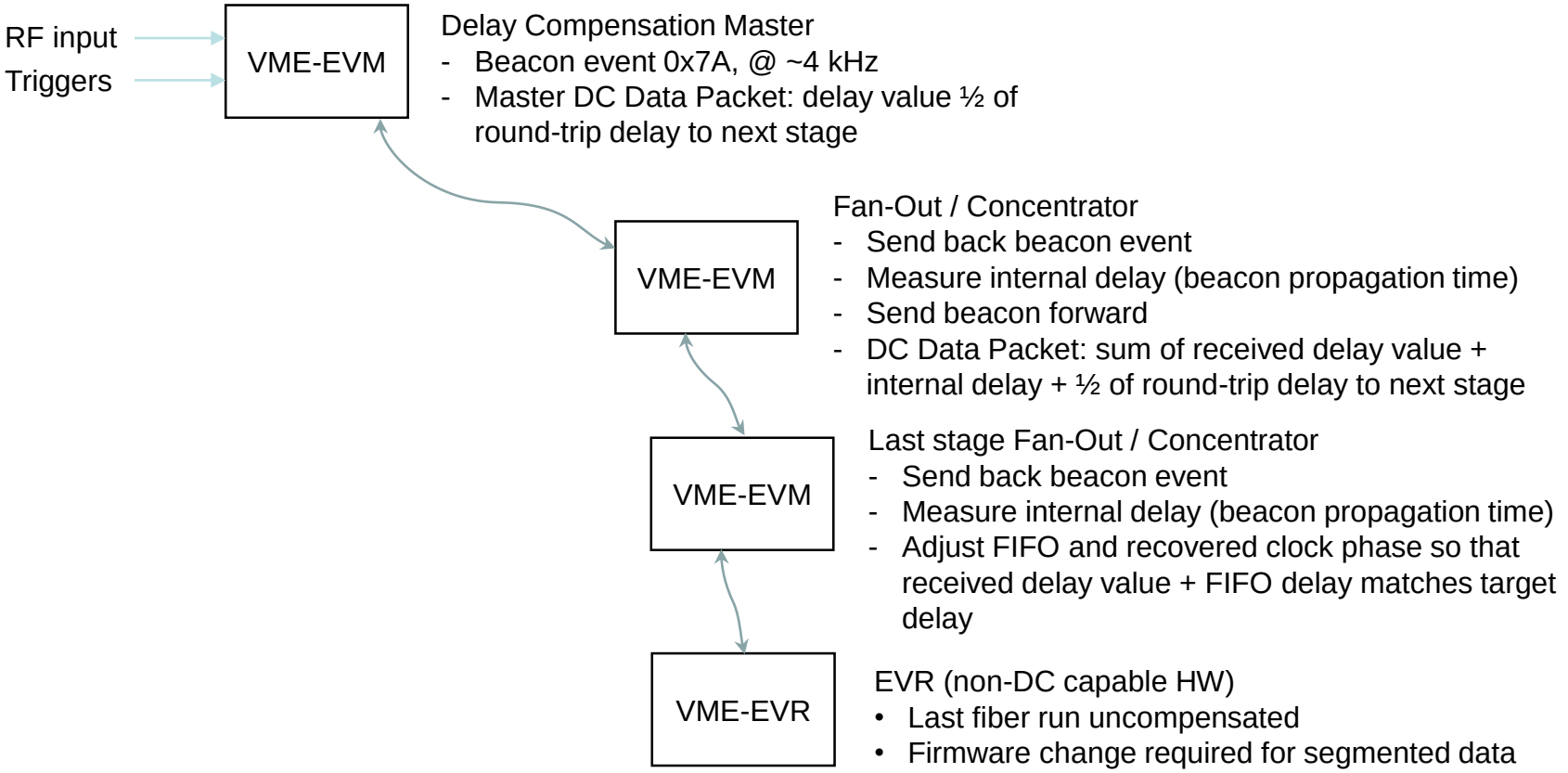
Timing System Topology with Delay Compensation



Delay Compensation

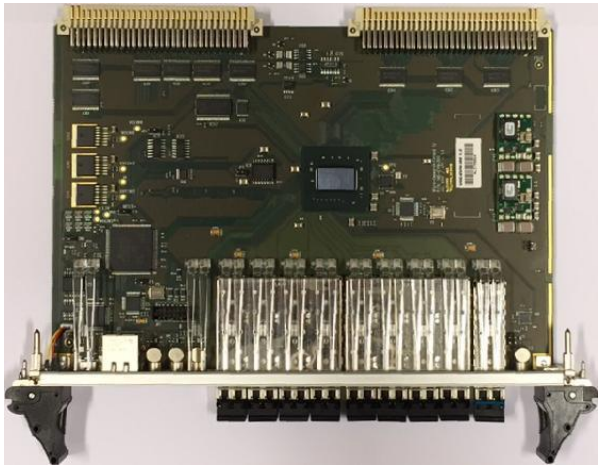


Delay Compensation for non-DC capable hardware



VME-EVM-300

- VME64x
- Event Generator
- 8-Way Fan-Out / Concentrator
- Event clock up to 142,9 MHz (room for improvement left)



- Integrated Fan-Out Concentrator and Event Generator
  - Reference clock from RF input or recovered clock from upstream EVM
  - Allows for fully synchronized downstream EVGs
- Masked events in Sequencer
  - Hardware or software mask/enable
- Segmented Data Buffer
  - 128 segments of 16 bytes each (2 kbyte buffer)

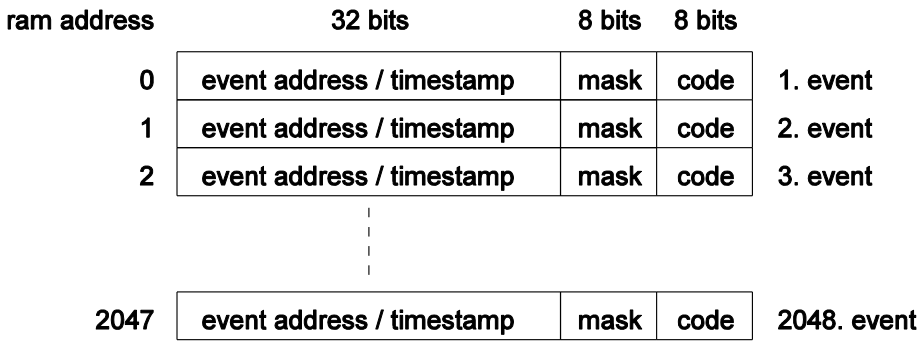
VME-EVR-300

- VME64x
- Event Receiver
- Four Universal I/O Slots (one slot driven by GTX)
- Two differential CML outputs (GTX)
- Two TTL inputs with default state selectable with jumpers
- Optional transition board VME-UNIV-TB64x

- Pulse Generator Triggers from prescalers and DBUS bits
- Gated pulse outputs
- Dual output mapping registers
- Segmented Data Buffer

Masked Sequencer Events

- New mask field in sequence RAM
- Four enable signals
  - When mask enable bit active ‘1’ enable event transmission only when HW signal active high or software mask enable bit active ‘1’
- Four disable signals
  - When mask disable bit active ‘1’ disable event transmission when HW signal active high or software mask disable bit active ‘1’



Segmented Data Buffer

- 128 segments of 16 bytes each (2 kbyte buffer)
- Segment 0x00 is reserved for Delay Compensation (delay value transmission)
- Transmission
  1. Write data into buffer
  2. Set up transmission: starting segment number, data length (may overlap several segment)
  3. Trigger transmission
- Receiving
  - Each segment has following flags (3 x 128 bits):
    - Receiving complete
    - Receiver overrun (segment overwritten before clearing receiving complete flag)
    - Checksum error
  - Interrupt may be enabled separately for each segment
  - Flags set only for starting segment

- Changes:
  - Receiver is always “armed” – no need to enable after a single data buffer reception
  - Protocol change due to segment number

EVR Gates and Dual Output Mapping Registers

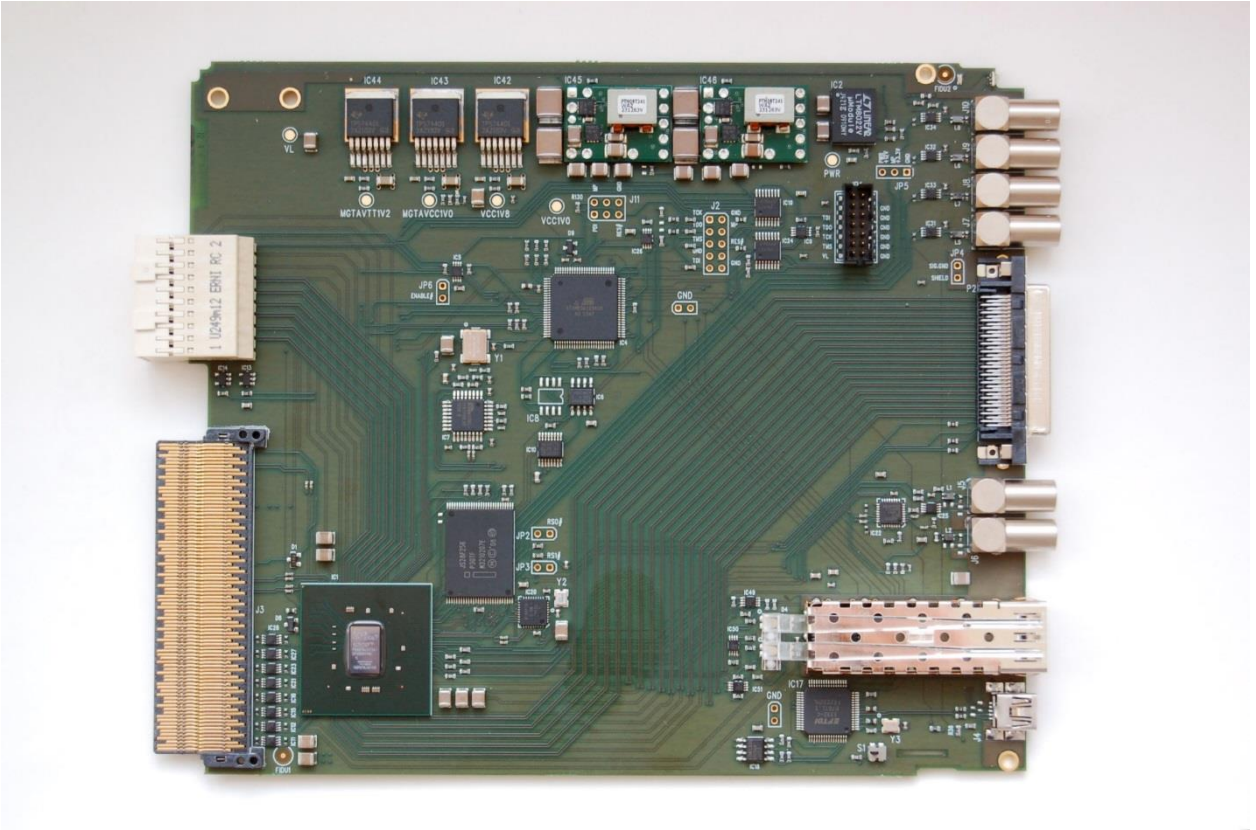
- Up to eight pulse generators operate as gates (masks and pulse enables)
- Gate state can be changed by
  - Events
  - Software
  - External signal by generating an external event
- Gates can be used to enable or disable pulse generators
- Each output mapping register now supports combining two sources (logical OR)
- This allows for:
  - “Switching” pulse generators (or pulse parameters) on event e.g. displacing trigger based on machine state

Planned EVM/EVR 02xx Firmware Features

- Integrate Downstream Event Receiver into EVM
  - Map pulse triggers to EVG inputs e.g. Sequencer control
- Integrate Upstream Event Receiver into EVM
- Control over Ethernet interface

MicroTCA.4 Event Receiver Prototype

- Production version by end of 2015



Products nearing end-of-life

Virtex II Pro based products nearing end-of-life:

- VME-EVG-230, VME-EVR-230, VME-EVR-230RF
  - Replaced by VME-EVM-300 and VME-EVR-300
- cPCI-EVG-230 and cPCI-EVR-230
- PMC-EVR-230

Low volume products:

- PXIe-EVR-300 / PXIe-EVG-300
- cPCI-EVRTG-300 (design has obsolete parts)